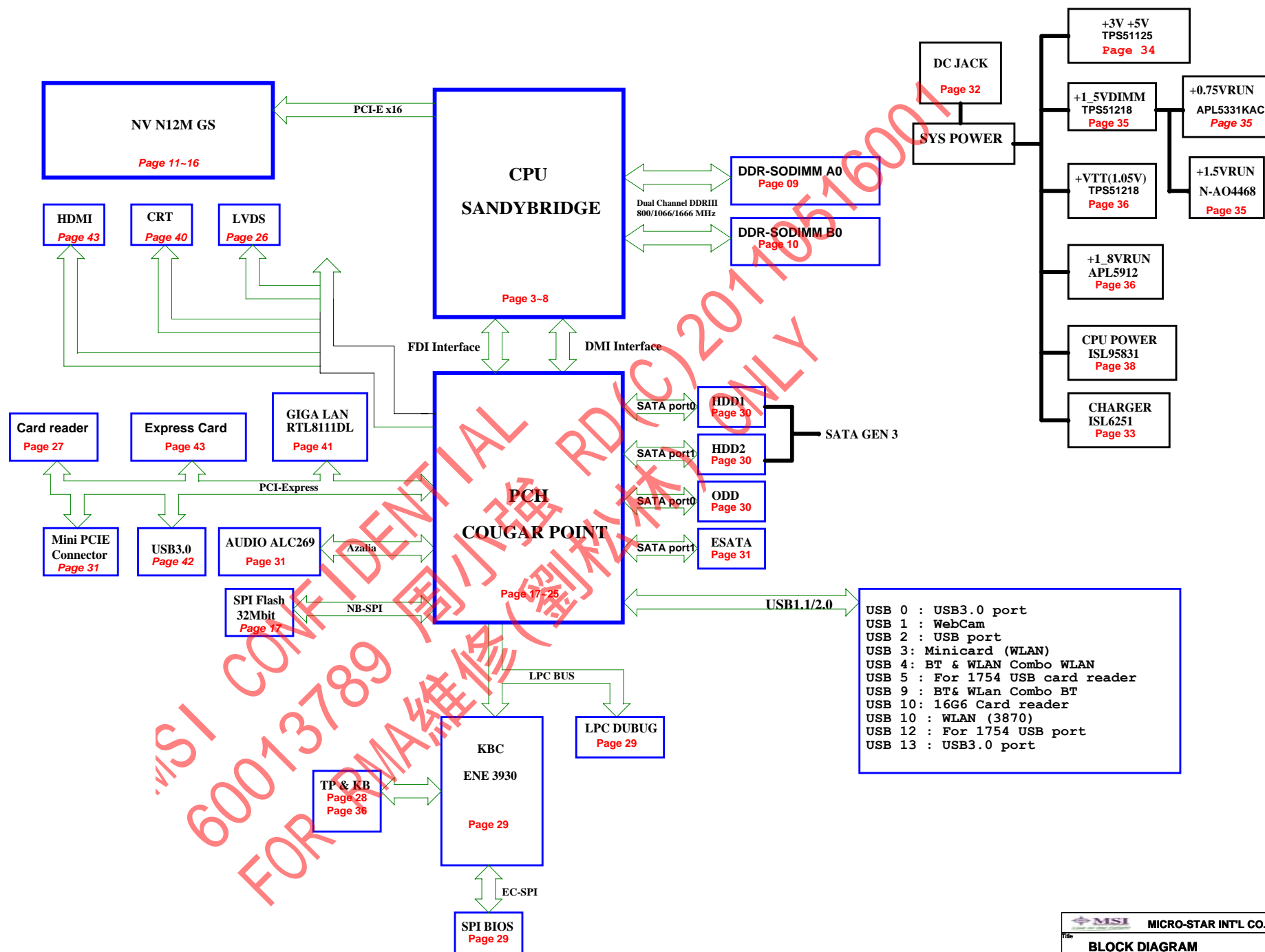


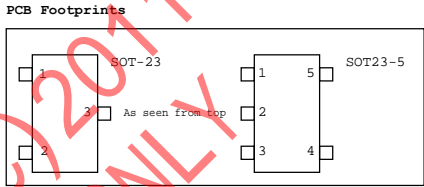
## Huron River Platform



SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

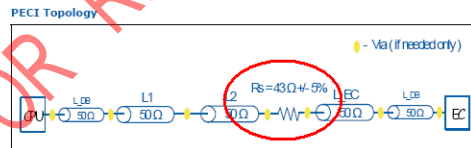
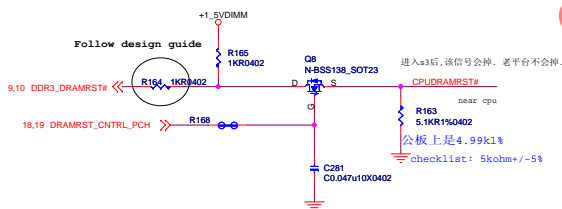
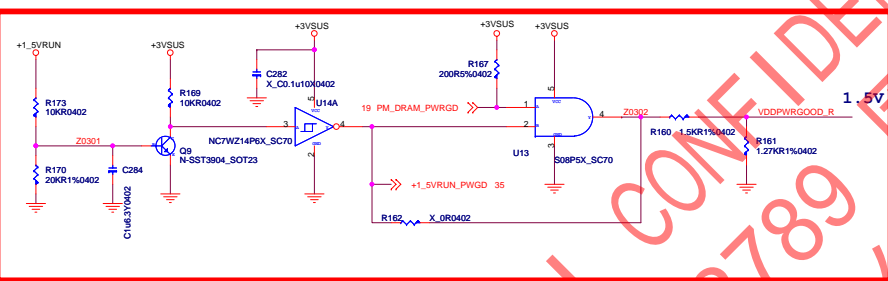
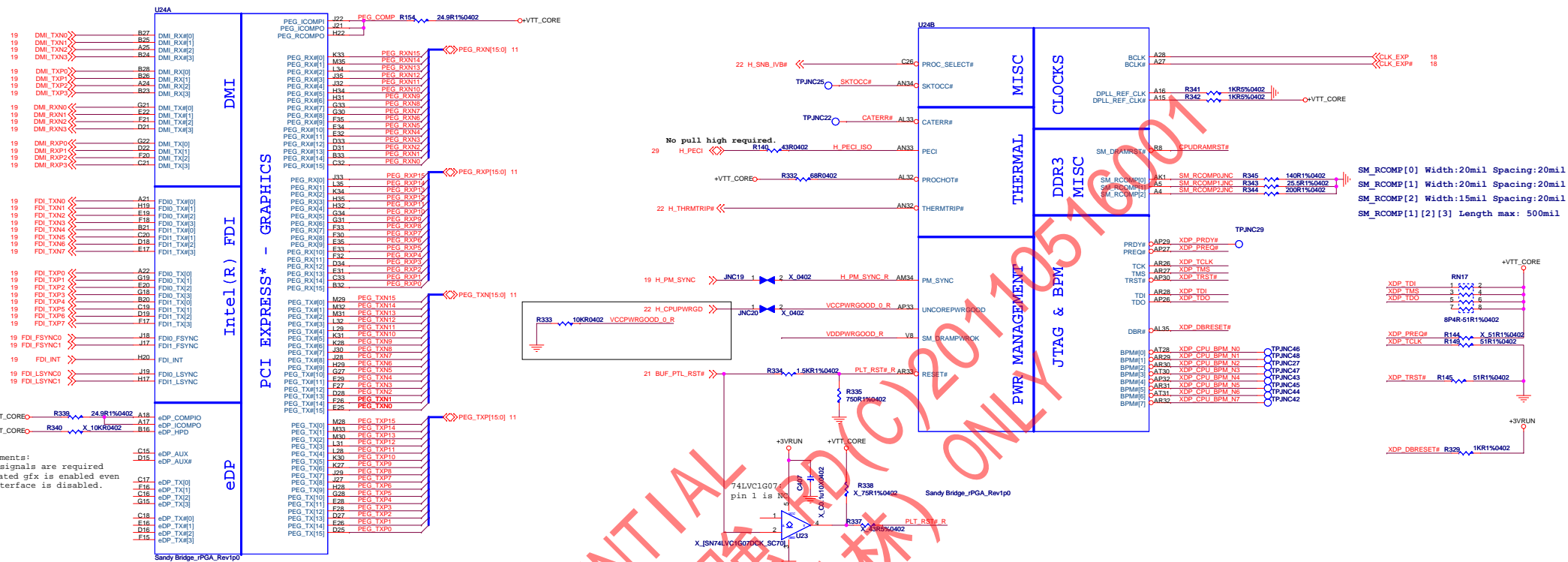
Voltage Rails			
POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
PWR_SRC	12V	S0, (S3-S5)	
+5VALW	5V	S0, (S3-S5)	
+5VRUN	5V	S0, S3	
+5VSUS	5V	S0	
+3VALW	3.3V	S0, (S3-S5)	
+3VRUN_CK505	3.3V	S0	Clock, MCH
+3VSUS	3.3V	S0, S3	
+3VRUN	3.3V	S0	
+1_5VDIMM	1.5V	S0, (S3-S4)	DDR core
+1_5VSUS	1.5V	S0	
+1_5VRUN	1.5V	S0	
VTT	1.05V	S0	PCH
+0_75VRUN	0.75V	S0	DDR command & control pull up.
+VCC_CORE	1.05V-1.1V	S0	CPU core rail
+VCC_GFXCORE	1.1V	S0	GMCH Graphics core rail

Net Naming Conventions	
Suffix	
# = Active Low Signal	
Prefix	
H = Host	
M = DDR Memory	
TP = Test Point (does not connect anywhere else)	

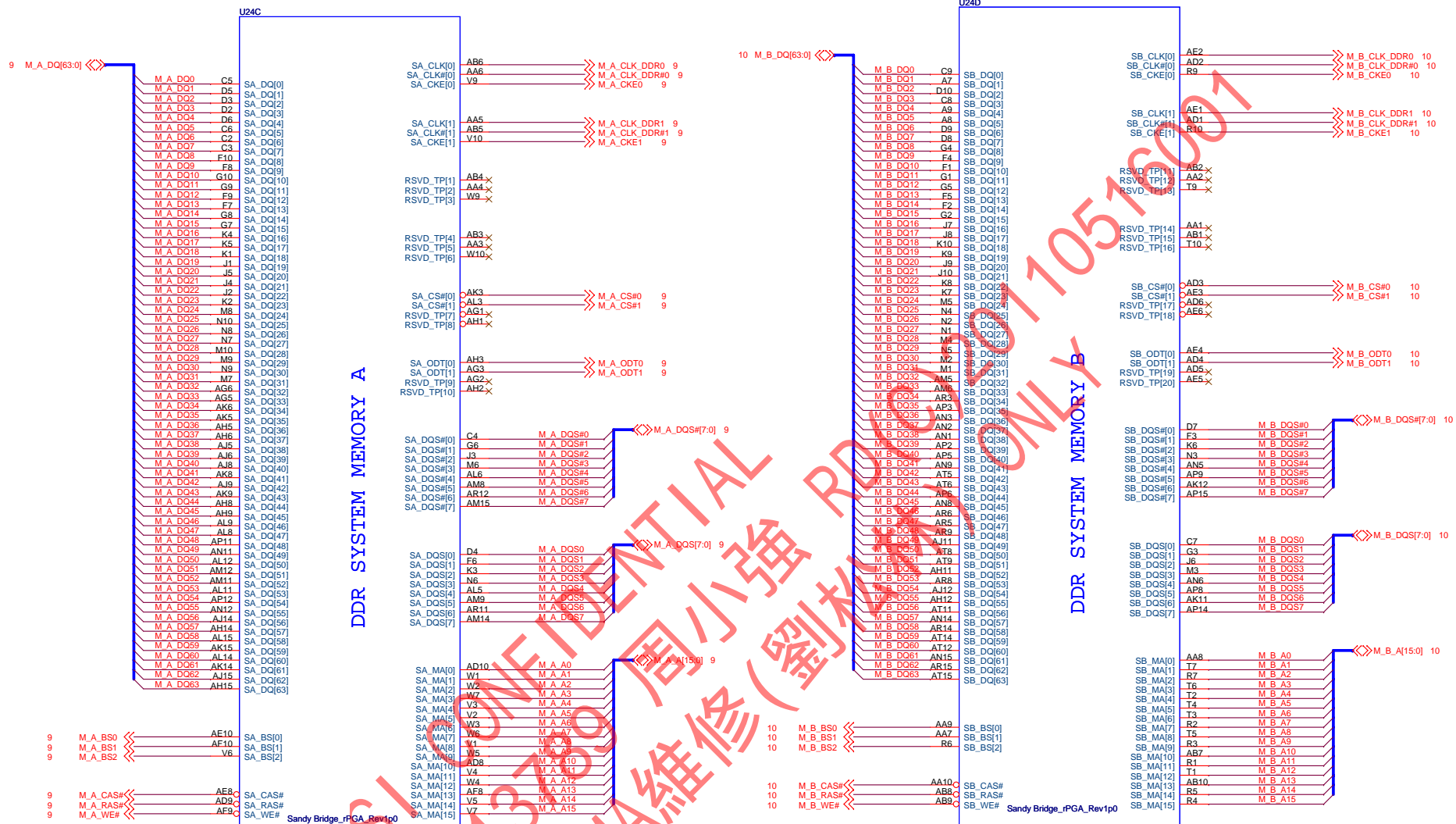


Power States	SLP S3#	SLP S4#	SLP S5#	+V*ALWAYS	+V*SUS	+V*RUN	CDR
S0 (Full on)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	ON	OFF	OFF	OFF

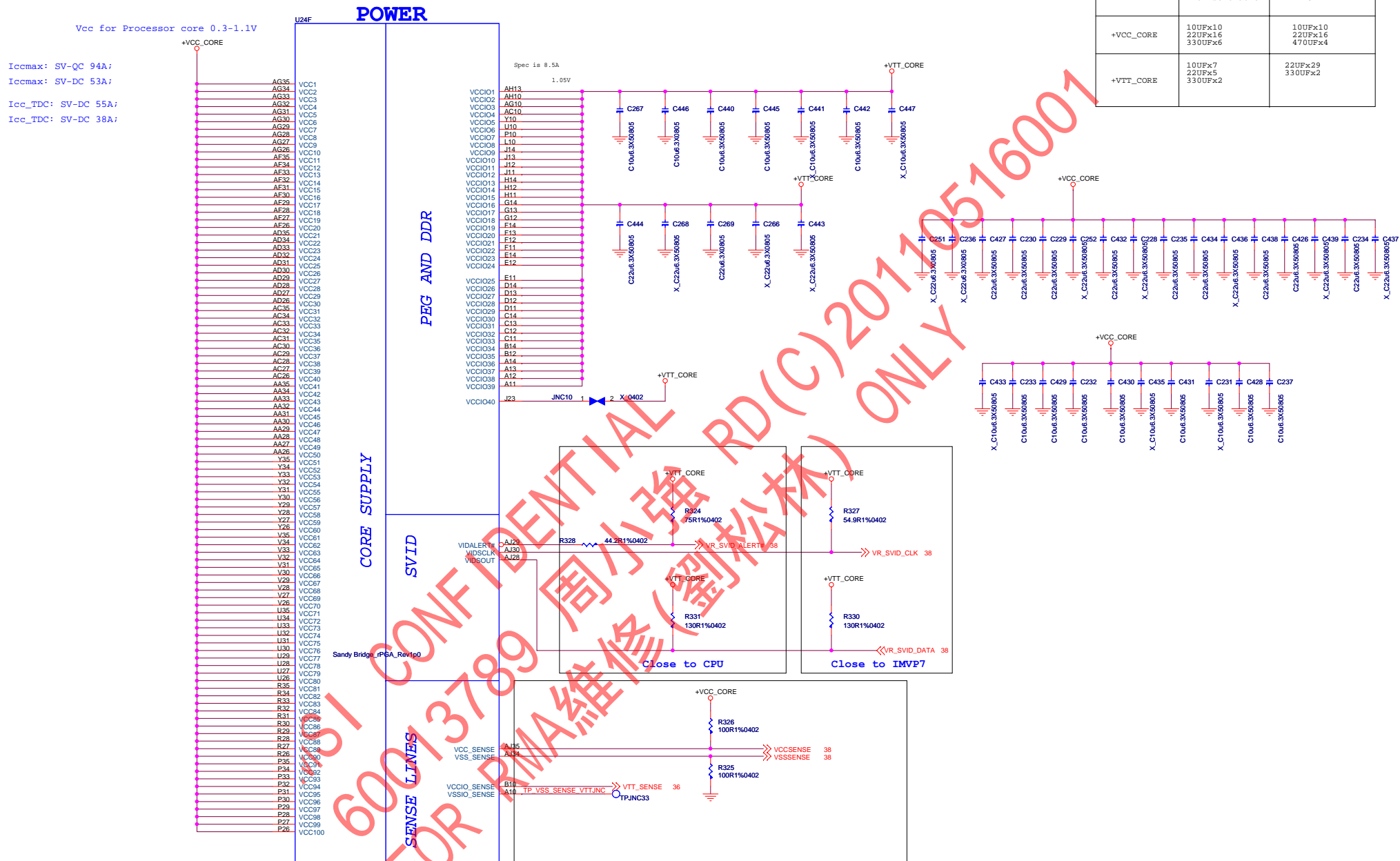
## SANDYBRIDGE PROCESSOR (CLK,MISC,JTAG)



# SANDYBRIDGE PROCESSOR (DDR3)

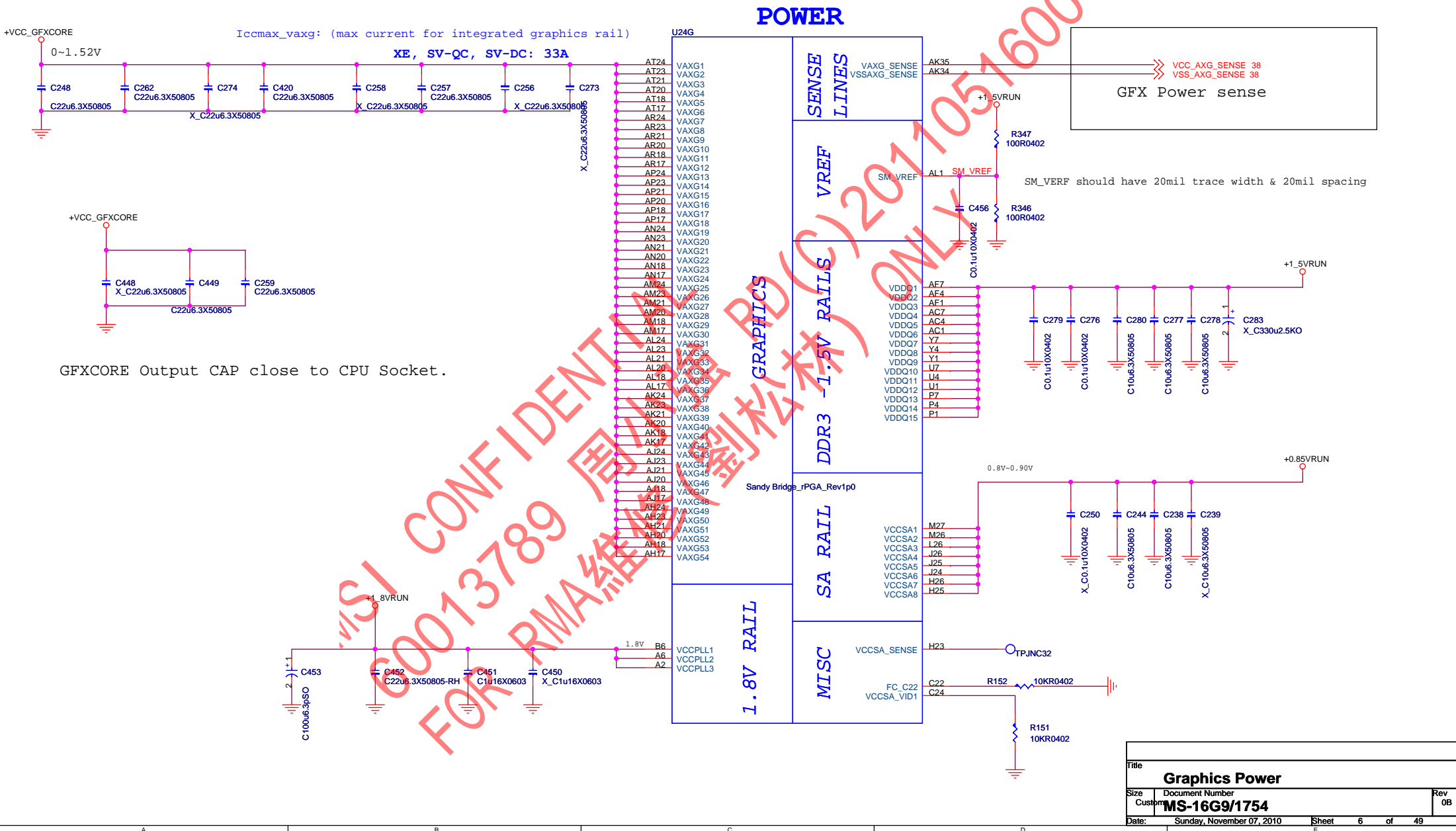


## SANDYBRIDGE PROCESSOR (POWER)

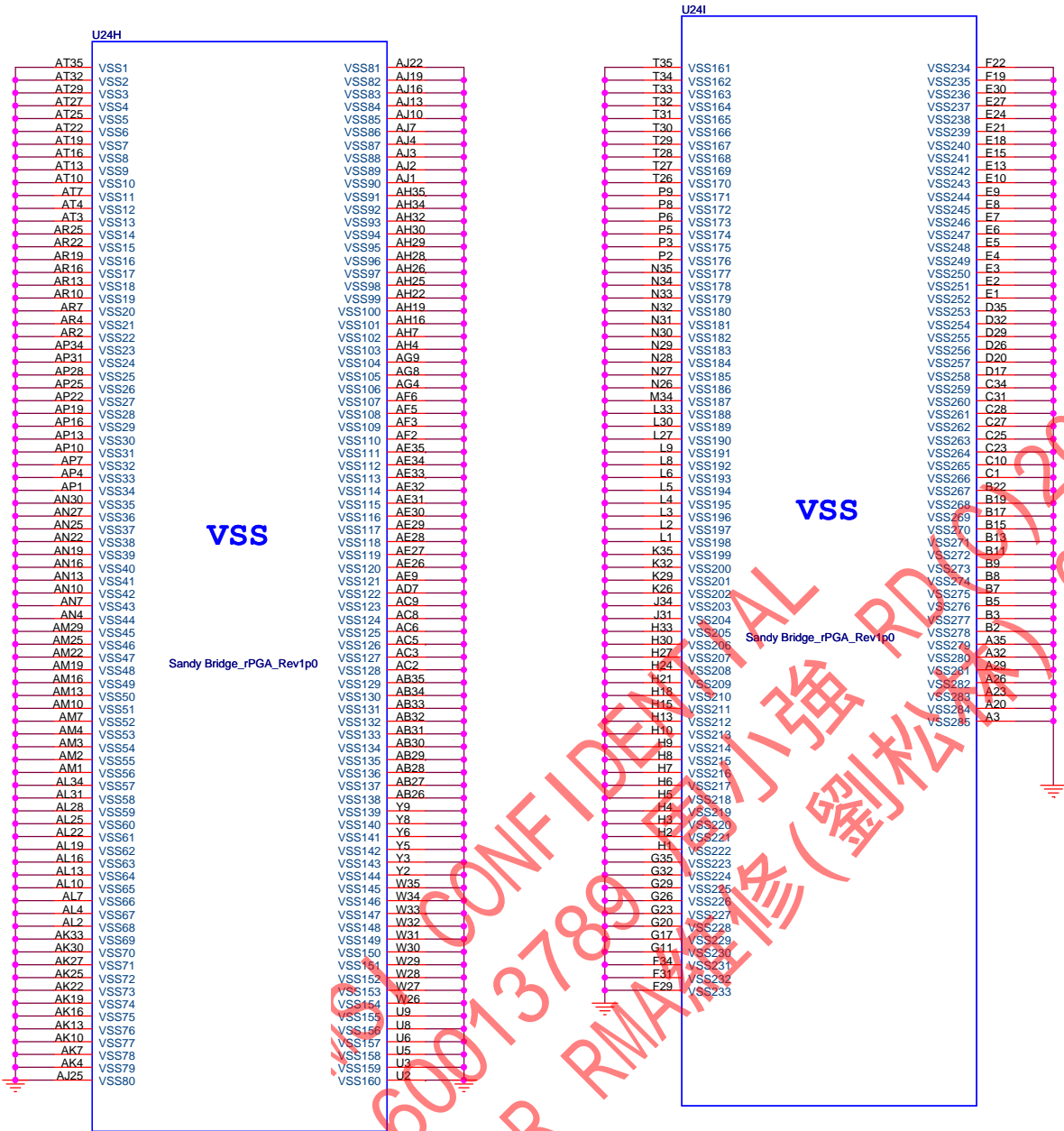


	148X schematic	CRB
+VCC_CORE	10UFx10 22UFx16 330UFx6	10UFx10 22UFx16 470UFx4
+VTT_CORE	10UFx7 22UFx5 330UFx2	22UFx29 330UFx2

SANDYBRIDGE PROCESSOR (GRAPHICS POWER)



SANDYBRIDGE PROCESSOR (GND)





SANDYBRIDGE PROCESSOR (RESERVED)

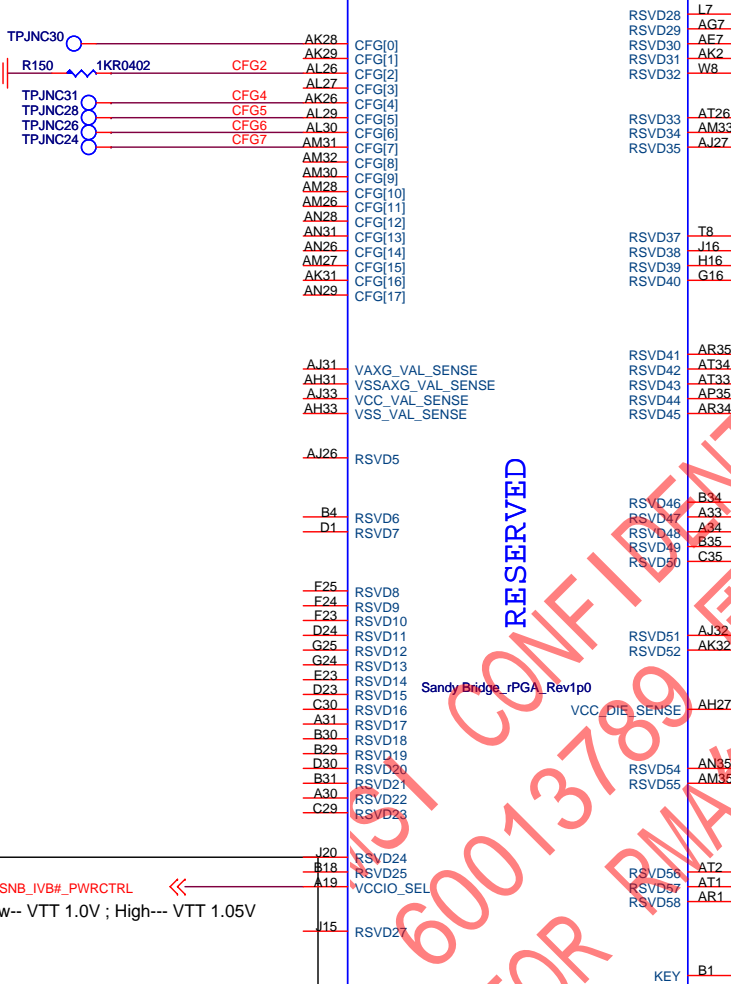
The CFG signals have a default value of "1" if not terminated on the board.

CFG2- PCI-Express Static Lane Reversal

CFG2

1 : Normal Operation  
0 : Lane Numbers Reversed  
15 -> 0, 14 -> 1, ...

U24E



CFG3- PCI-Express Static Lane Reversal	
CFG2	1 : Normal Operation 0 : Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

PCI-Express Configuration Select	
CFG[5:6]	11: Default X16-device 1 functions 1 and 2 disabled 10: X8 X8-device 1 functions 1 enable, function2 disabled 01: Reserved--(device 1 functions 1 disabled function2 enable 00: X8 X4 X4-device 1 functions 1 and 2 enable

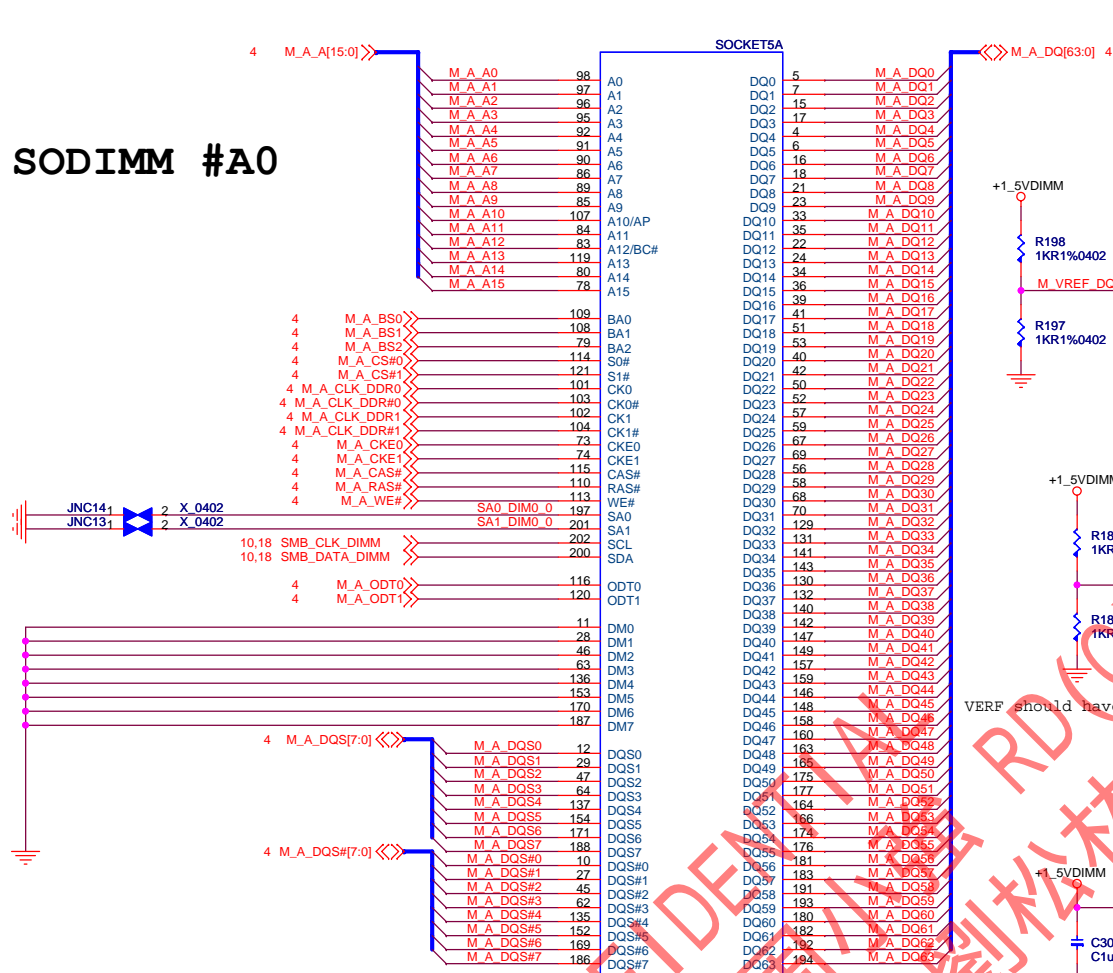
PEG DEFER TRAINING	
CFG7	1 : (Default) PEG train immediately following xxRESETB de assertion 0 : PEG wait for BIOS for training

DATASHEET 记录	
CFG[17:7]	Reserved configuration lanes. A test point may be placed on the board for these lands.

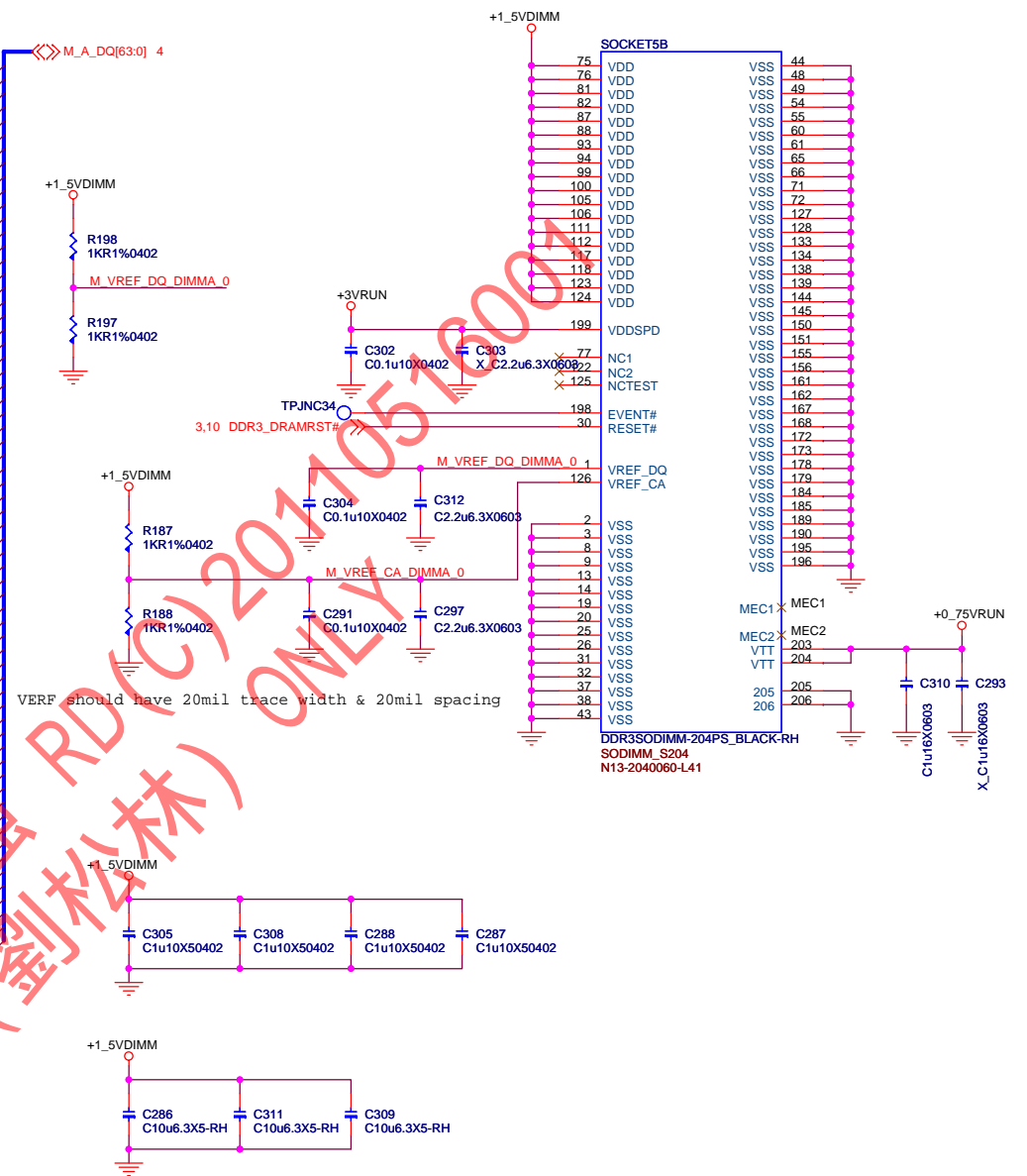
Title		
PROCESSOR RESERVED		
Size	Document Number	Rev
Custom	MS-16G9/1754	0B
Date:	Sunday, November 07, 2010	Sheet 8 of 49



# SODIMM #A0



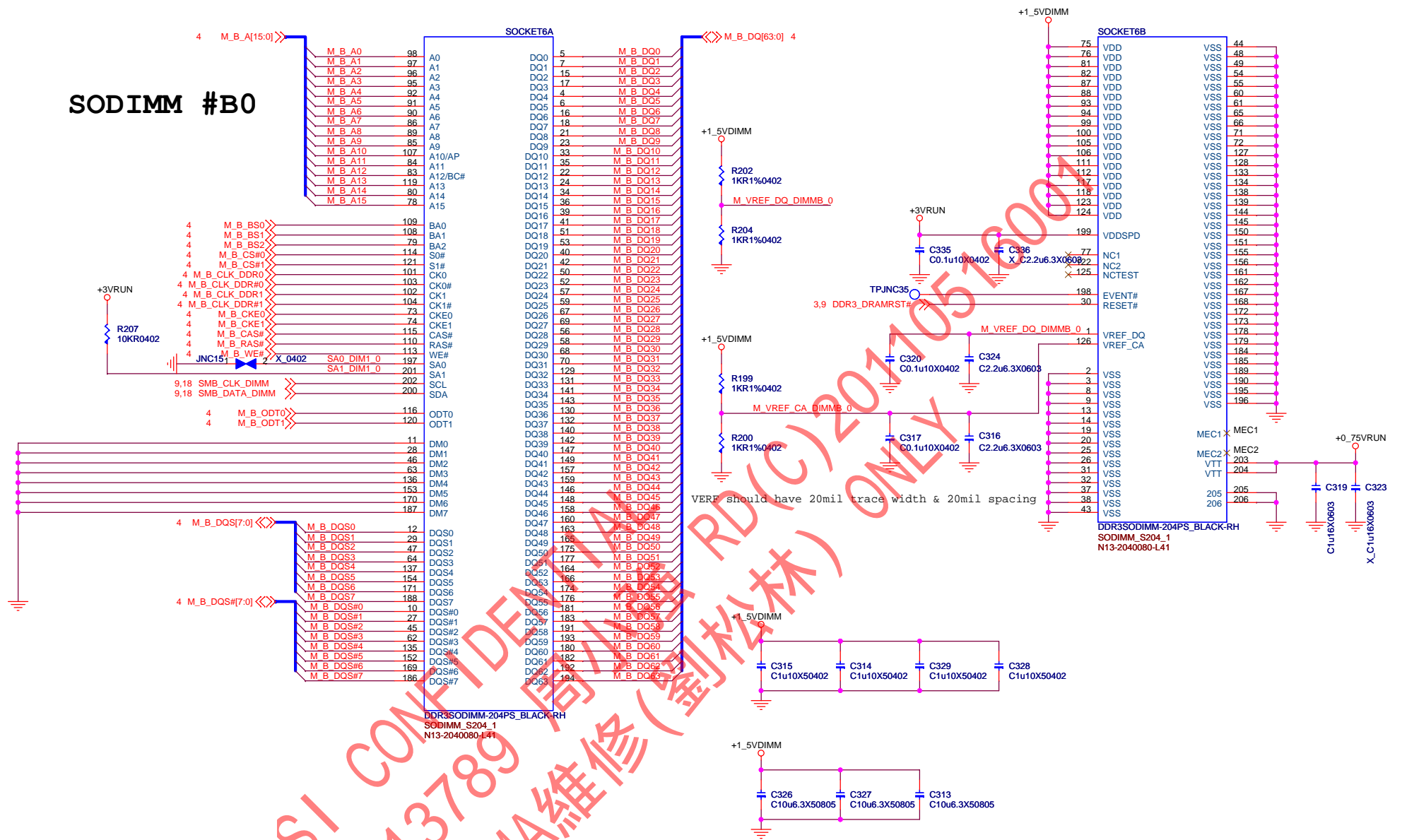
DDR3SODIMM-204PS\_BLACK-RH  
SODIMM\_S204  
N13-2040060-L41



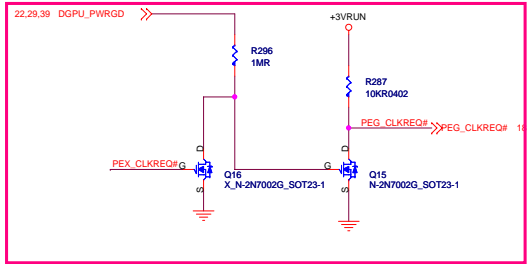
VERF should have 20mil trace width & 20mil spacing

Title			
DDR3 SODIMM A0			
Size	Document Number		Rev
Customer	MS-16G9/1754		OB
Date:	Sunday, November 07, 2010	Sheet	9 of 49

# SODIMM #B0



Title					
DDR3 SODIMM B0					
Size	Document Number				Rev 0B
Customer	MS-16G9/1754				
Date:	Sunday, November 07, 2010	Sheet	10	of	49



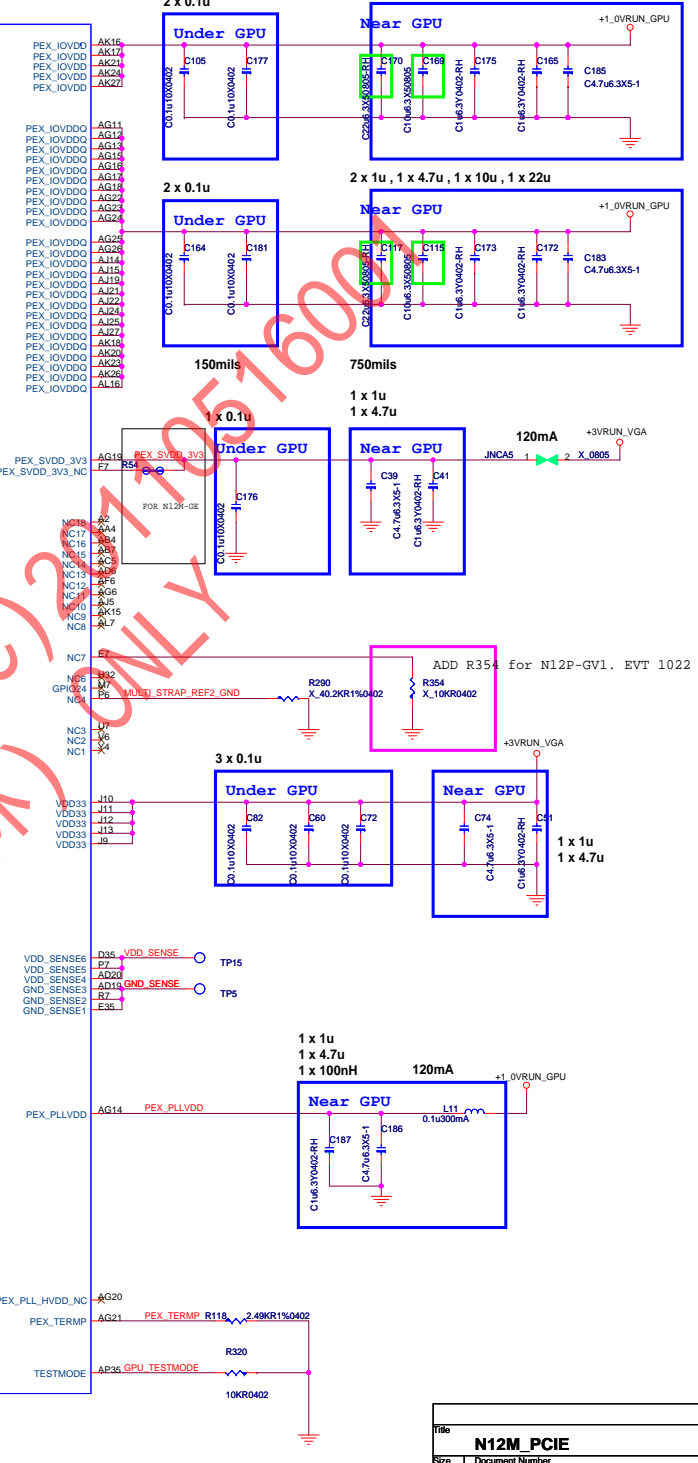
PEG\_RXN[15:0] << PEG\_RXN[15:0] 3  
PEG\_RXP[15:0] << PEG\_RXP[15:0] 3  
PEG\_TXP[15:0] << PEG\_TXP[15:0] 3  
PEG\_TXN[15:0] << PEG\_TXN[15:0] 3

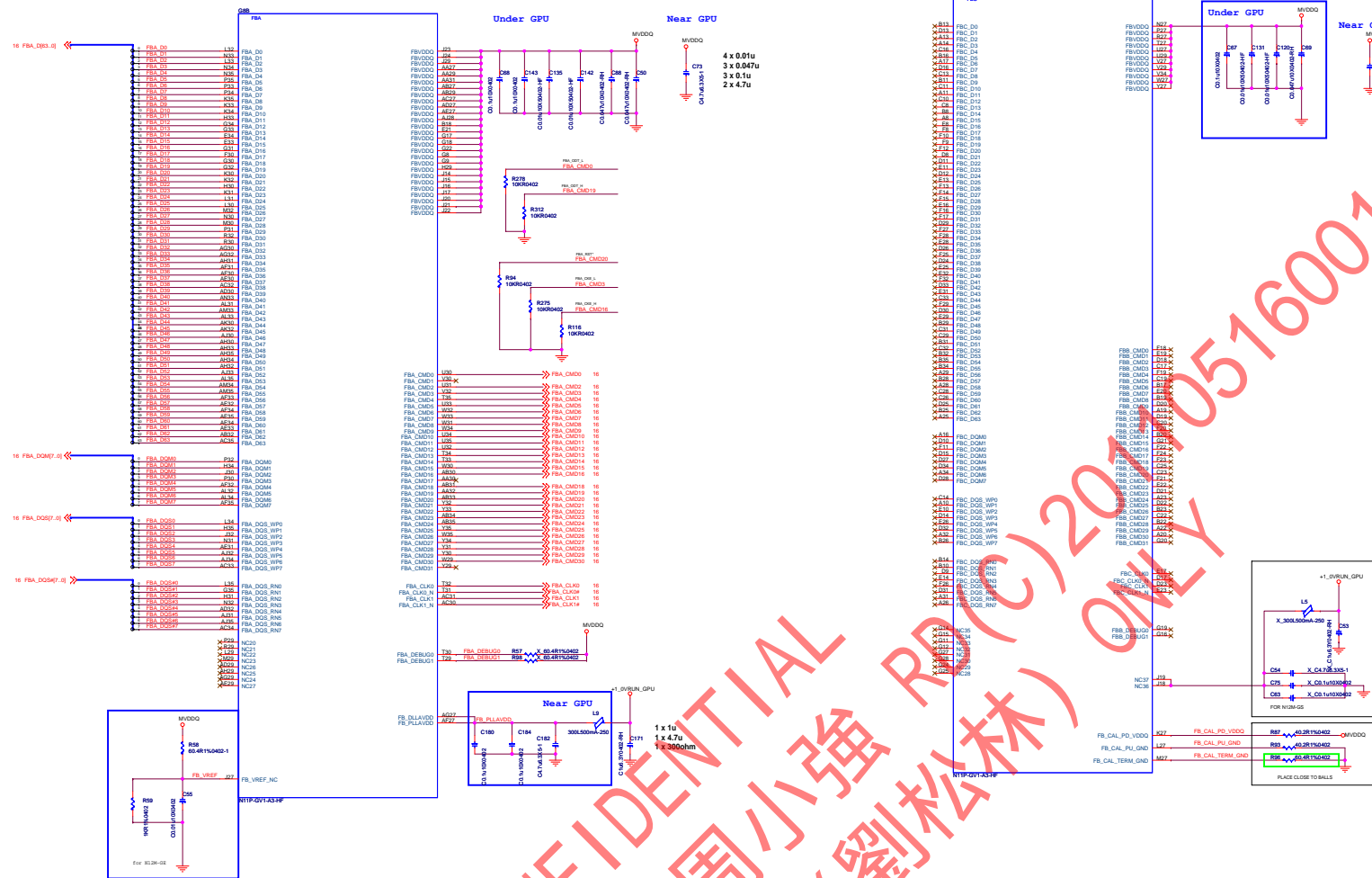
PEG\_TXN0 C0.1u10X0402 C424 PEG\_C\_TXN0JNC  
PEG\_TXN1 C0.1u10X0402 C422 PEG\_C\_TXN1JNC  
PEG\_TXN2 C0.1u10X0402 C419 PEG\_C\_TXN2JNC  
PEG\_TXN3 C0.1u10X0402 C417 PEG\_C\_TXN3JNC  
PEG\_TXN4 C0.1u10X0402 C411 PEG\_C\_TXN4JNC  
PEG\_TXN5 C0.1u10X0402 C408 PEG\_C\_TXN5JNC  
PEG\_TXN6 C0.1u10X0402 C403 PEG\_C\_TXN6JNC  
PEG\_TXN7 C0.1u10X0402 C401 PEG\_C\_TXN7JNC  
PEG\_TXN8 C0.1u10X0402 C399 PEG\_C\_TXN8JNC  
PEG\_TXN9 C0.1u10X0402 C387 PEG\_C\_TXN9JNC  
PEG\_TXN10 C0.1u10X0402 C389 PEG\_C\_TXN10JNC  
PEG\_TXN11 C0.1u10X0402 C381 PEG\_C\_TXN11JNC  
PEG\_TXN12 C0.1u10X0402 C383 PEG\_C\_TXN12JNC  
PEG\_TXN13 C0.1u10X0402 C386 PEG\_C\_TXN13JNC  
PEG\_TXN14 C0.1u10X0402 C385 PEG\_C\_TXN14JNC  
PEG\_TXN15 C0.1u10X0402 C385 PEG\_C\_TXN15JNC

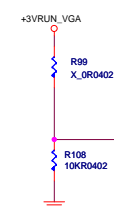
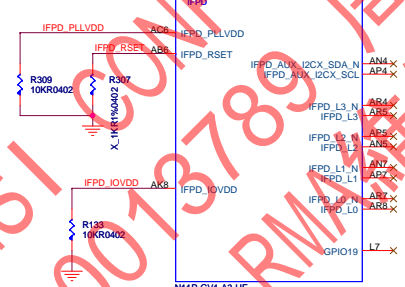
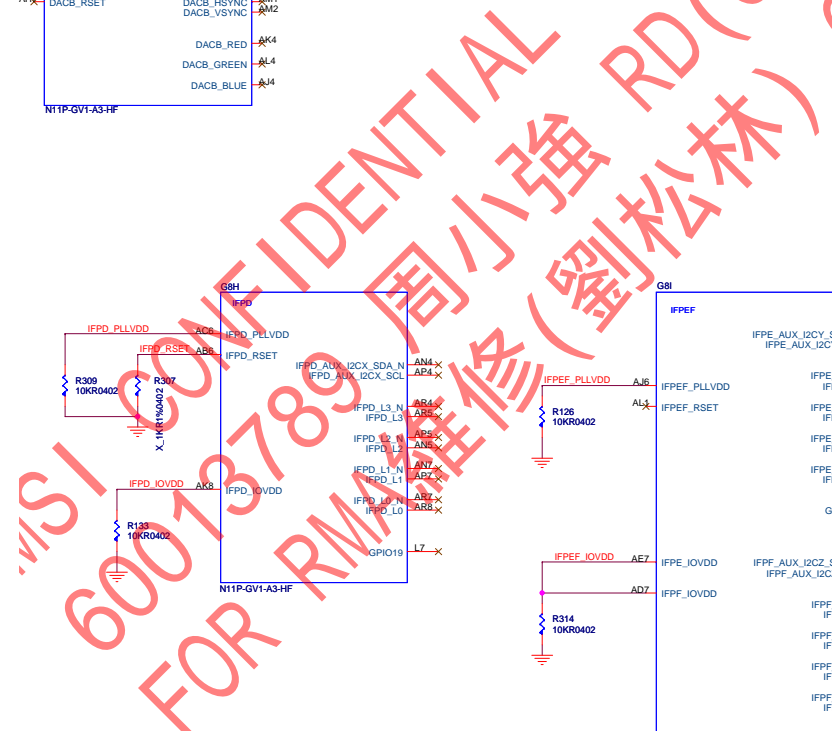
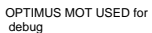
PEG\_TXP0 C0.1u10X0402 C425 PEG\_C\_TXP0JNC  
PEG\_TXP1 C0.1u10X0402 C423 PEG\_C\_TXP1JNC  
PEG\_TXP2 C0.1u10X0402 C421 PEG\_C\_TXP2JNC  
PEG\_TXP3 C0.1u10X0402 C418 PEG\_C\_TXP3JNC  
PEG\_TXP4 C0.1u10X0402 C416 PEG\_C\_TXP4JNC  
PEG\_TXP5 C0.1u10X0402 C410 PEG\_C\_TXP5JNC  
PEG\_TXP6 C0.1u10X0402 C404 PEG\_C\_TXP6JNC  
PEG\_TXP7 C0.1u10X0402 C402 PEG\_C\_TXP7JNC  
PEG\_TXP8 C0.1u10X0402 C400 PEG\_C\_TXP8JNC  
PEG\_TXP9 C0.1u10X0402 C398 PEG\_C\_TXP9JNC  
PEG\_TXP10 C0.1u10X0402 C396 PEG\_C\_TXP10JNC  
PEG\_TXP11 C0.1u10X0402 C388 PEG\_C\_TXP11JNC  
PEG\_TXP12 C0.1u10X0402 C380 PEG\_C\_TXP12JNC  
PEG\_TXP13 C0.1u10X0402 C382 PEG\_C\_TXP13JNC  
PEG\_TXP14 C0.1u10X0402 C385 PEG\_C\_TXP14JNC  
PEG\_TXP15 C0.1u10X0402 C394 PEG\_C\_TXP15JNC

PEG\_RXN0 C202 C0.1u10X0402 PEG\_RXN0\_CJNC  
PEG\_RXN1 C210 C0.1u10X0402 PEG\_RXN1\_CJNC  
PEG\_RXN2 C198 C0.1u10X0402 PEG\_RXN2\_CJNC  
PEG\_RXN3 C211 C0.1u10X0402 PEG\_RXN3\_CJNC  
PEG\_RXN4 C195 C0.1u10X0402 PEG\_RXN4\_CJNC  
PEG\_RXN5 C209 C0.1u10X0402 PEG\_RXN5\_CJNC  
PEG\_RXN6 C191 C0.1u10X0402 PEG\_RXN6\_CJNC  
PEG\_RXN7 C205 C0.1u10X0402 PEG\_RXN7\_CJNC  
PEG\_RXN8 C194 C0.1u10X0402 PEG\_RXN8\_CJNC  
PEG\_RXN9 C219 C0.1u10X0402 PEG\_RXN9\_CJNC  
PEG\_RXN10 C207 C0.1u10X0402 PEG\_RXN10\_CJNC  
PEG\_RXN11 C223 C0.1u10X0402 PEG\_RXN11\_CJNC  
PEG\_RXN12 C215 C0.1u10X0402 PEG\_RXN12\_CJNC  
PEG\_RXN13 C221 C0.1u10X0402 PEG\_RXN13\_CJNC  
PEG\_RXN14 C214 C0.1u10X0402 PEG\_RXN14\_CJNC  
PEG\_RXN15 C226 C0.1u10X0402 PEG\_RXN15\_CJNC

PEG\_RXP0 C200 C0.1u10X0402 PEG\_RXP0\_CJNC  
PEG\_RXP1 C201 C0.1u10X0402 PEG\_RXP1\_CJNC  
PEG\_RXP2 C197 C0.1u10X0402 PEG\_RXP2\_CJNC  
PEG\_RXP3 C212 C0.1u10X0402 PEG\_RXP3\_CJNC  
PEG\_RXP4 C196 C0.1u10X0402 PEG\_RXP4\_CJNC  
PEG\_RXP5 C208 C0.1u10X0402 PEG\_RXP5\_CJNC  
PEG\_RXP6 C192 C0.1u10X0402 PEG\_RXP6\_CJNC  
PEG\_RXP7 C206 C0.1u10X0402 PEG\_RXP7\_CJNC  
PEG\_RXP8 C193 C0.1u10X0402 PEG\_RXP8\_CJNC  
PEG\_RXP9 C220 C0.1u10X0402 PEG\_RXP9\_CJNC  
PEG\_RXP10 C204 C0.1u10X0402 PEG\_RXP10\_CJNC  
PEG\_RXP11 C224 C0.1u10X0402 PEG\_RXP11\_CJNC  
PEG\_RXP12 C216 C0.1u10X0402 PEG\_RXP12\_CJNC  
PEG\_RXP13 C222 C0.1u10X0402 PEG\_RXP13\_CJNC  
PEG\_RXP14 C213 C0.1u10X0402 PEG\_RXP14\_CJNC  
PEG\_RXP15 C225 C0.1u10X0402 PEG\_RXP15\_CJNC

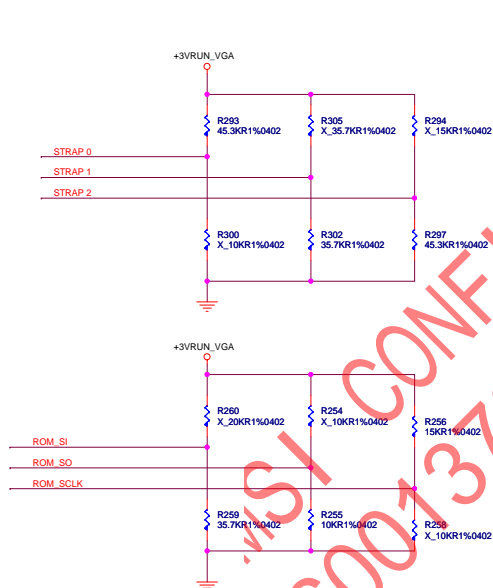
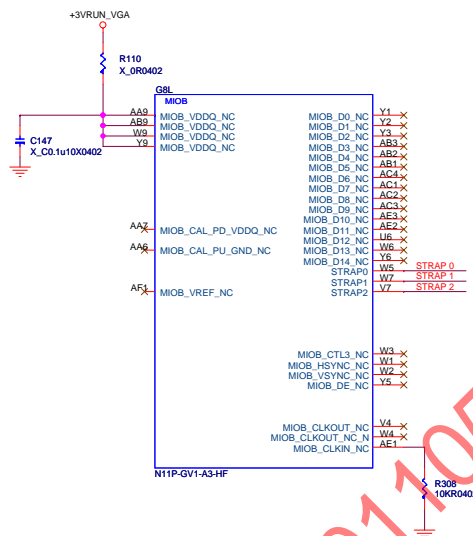
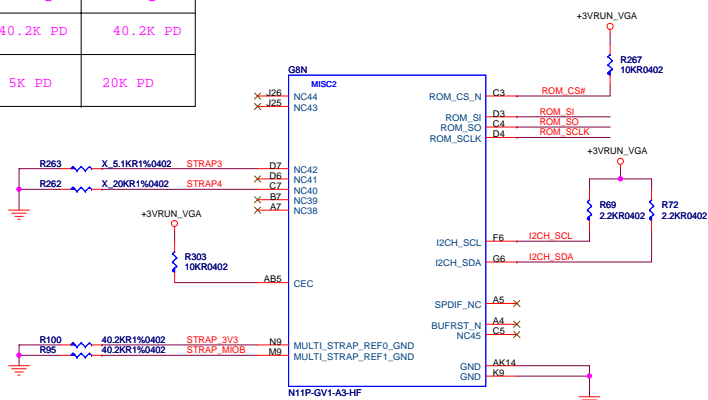








	Strap3	Strap4
N12M-GS1	40.2K PD	40.2K PD
N12P-GV1/GV	5K PD	20K PD



	N12M	USER 1	1	
		USER 2	1	
STRAP0		USER 1	1	SM BUS desine resolution 1111
PU 45K		USER 0	1	
		3G10_P1DCFG 1	0	
		3G10_P1DCFG 4	1	N12M-GS:PD 35K
STRAP1		3G10_P1DCFG 1	1	N12M-GE:PU 35K
PD 15K		3G10_P1DCFG 1	1	N12M-GS1:PD 35K
		3G10_P2PCFG 0	0	N12P-GV1: PD35K
		PCI_DEVID3	0	
		PCI_DEVID2	4	N12M-GS:PD 25K,
STRAP2		PCI_DEVID1	0	N12M-GE:PU 15K
		PCI_DEVID0	0/2	N12M-GS1: PU15K
				N12P-GV1: PD45K
		PCI DEVID	1	
		SHWVENDOR	0	N12M-GS:PU 15K,
ROM_SCLK		ROM_CTL	1	N12M-GE:PU 35K,
PU 15K		ROM_CTL_EN	0	N12M-GS1:PD 15K
		RAMCFG 3	0	
		RAMCFG 2	1	
ROM_SCLK		RAMCFG 1	1	Hynix 128Mx16----- PD35K
PD 15K		RAMCFG 0	1	Samsung 128Mx16----- PD45K
		XCCLK_417	0	
ROM_SO		FB_0_BAR_SIZE	0	Have 27M hz CRYSTAL
PD 10K		SMB_ALT_ADDR	0	FB Aperture size 256MB
		VGA_DEVICE	1	0X9E(Default , not Multi-GPU usage)
				VGA Device

Rvalue	PU	PD
5K	1000	000
10K	1001	000
15K	1010	001
20K	1011	001
25K	1100	010
30K	1101	010
35K	1110	011
45K	1111	011





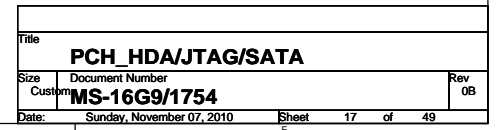
**Flash Descriptor Security Protect**

HDA_SDO	Low = Enable High = Disable
TPJNC39	
TPJNC9	
TPJNC10	
TPJNC38	

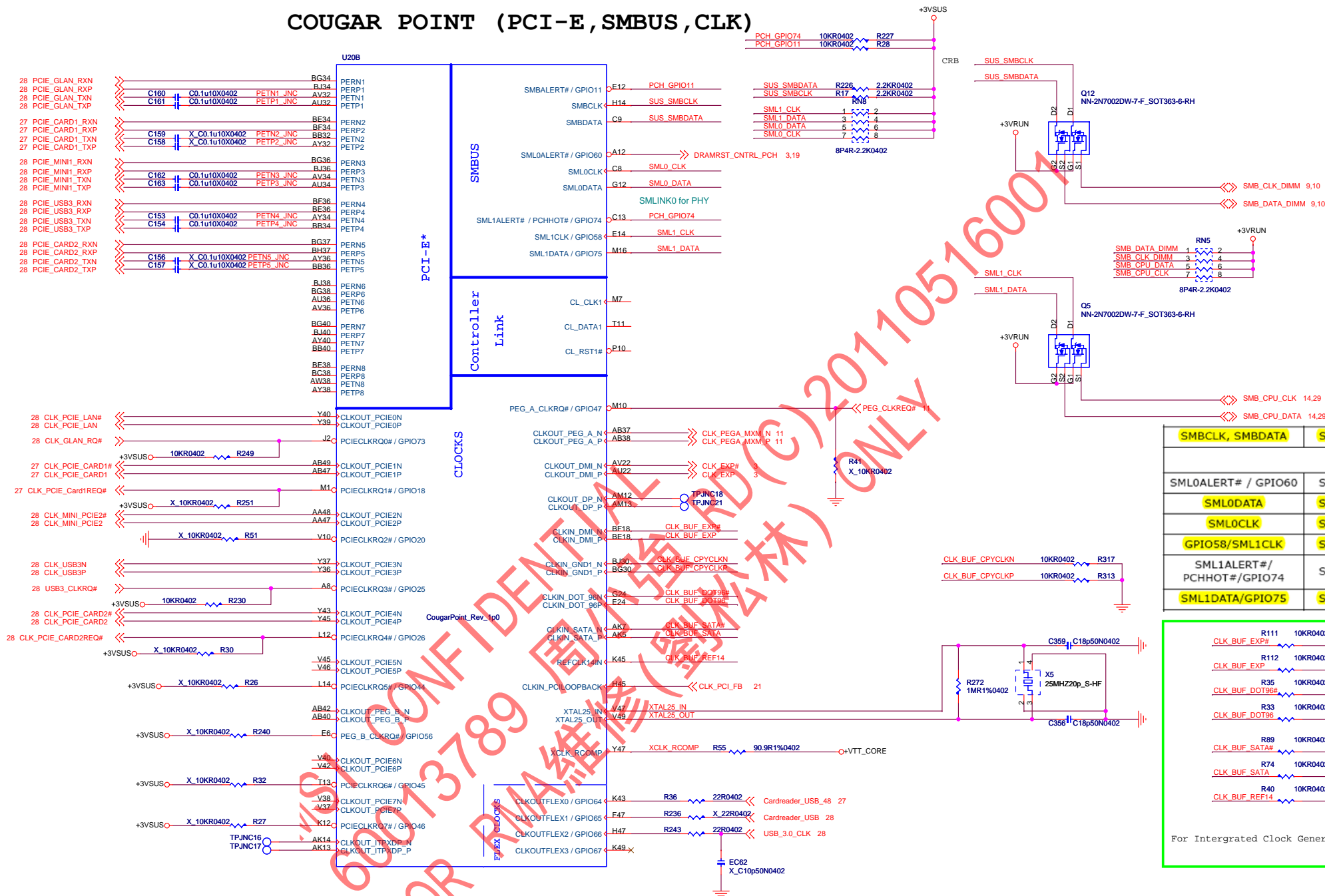
Unused SATAxGP pins must be terminated

close to the

2010/01/07 for EMI request change page



## COUGAR POINT (PCI-E, SMBUS, CLK)

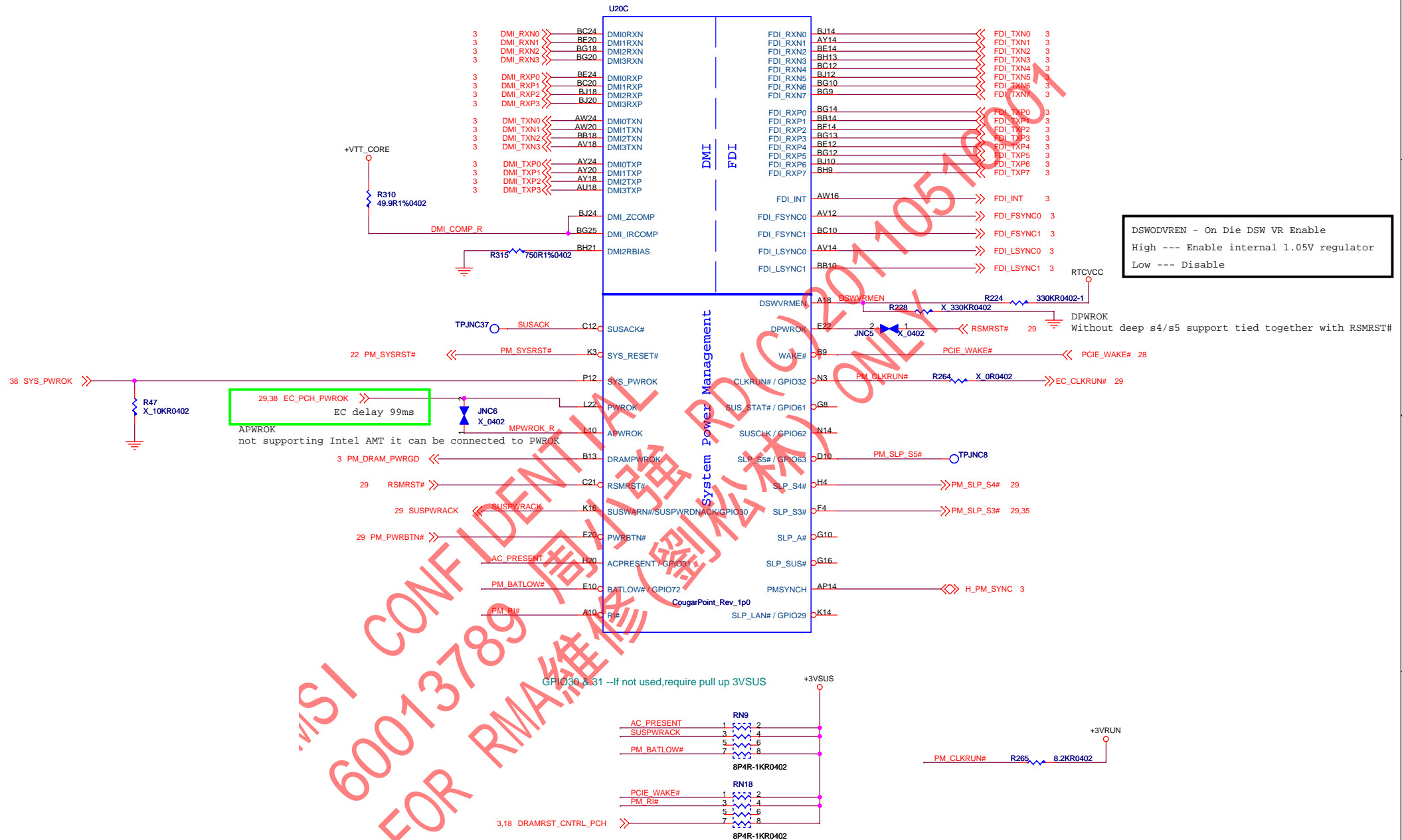


NOTE: If CLKREQ# control is not needed, say for a free running clock, do not pull-down signal to GND. This will increase leakage in Sx states. A 10 kohms±5% external pull-up resistor still needs to be used, but the corresponding CLKREQ# function can be disabled via Intel® Management Engine (Intel® ME) FW. Please refer to Intel ME FW Bring Up Guide for configuring/disabling CLKREQ#.

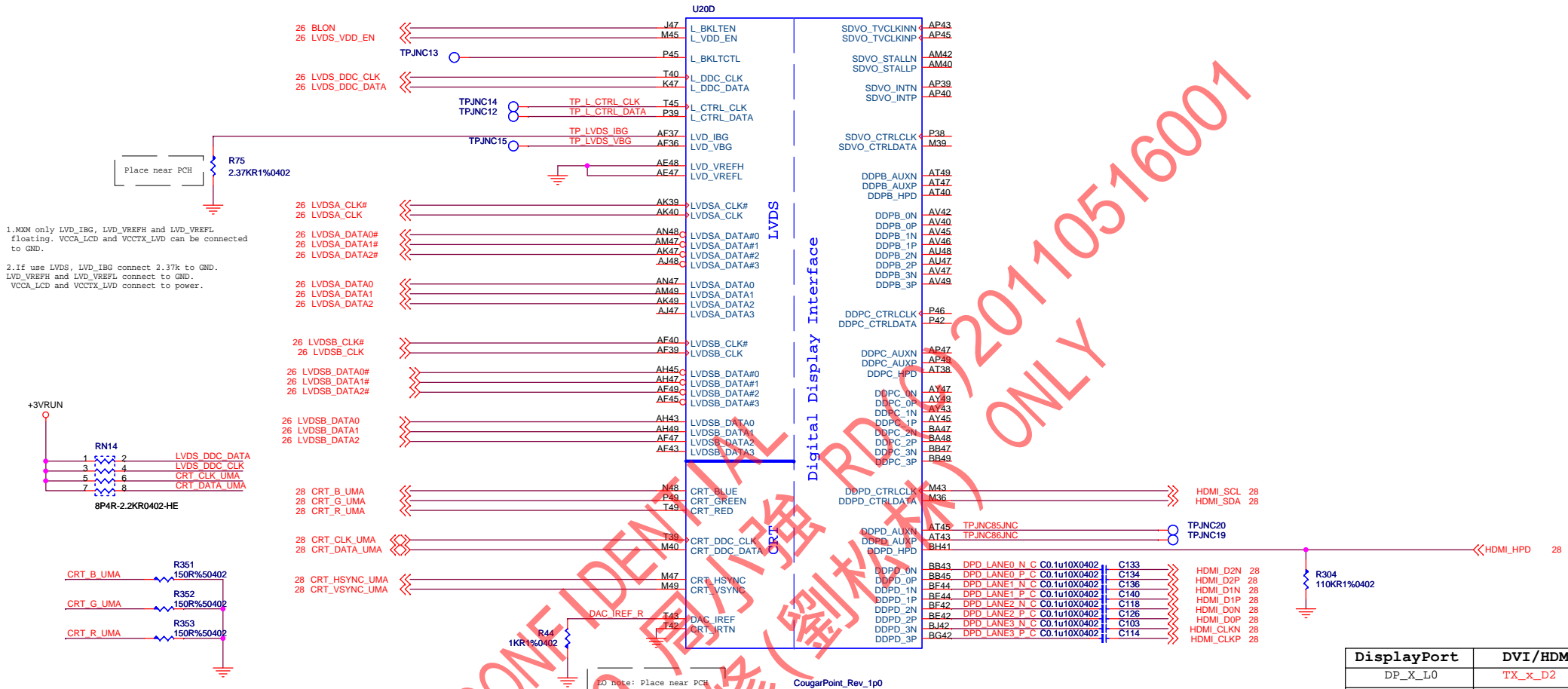
Only PCIECLKRQ[2:1]# on PCH are core well powered. All other PCIECLKRQx# are suspend well powered.

Title				
<b>PCH_PCIE/SMBUS/CLK</b>				
Size	Document Number			Rev
Customer	<b>MS-16G9/1754</b>			<b>0B</b>
Date:	Sunday, November 07, 2010	Sheet	18	of 49

## COUGAR POINT (DMI, FDI, GPIO)

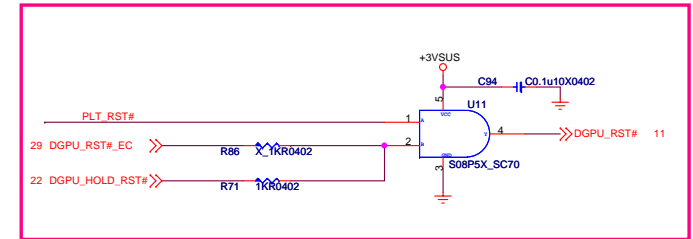


# COUGAR POINT (LVDS,DDI)



DisplayPort	DVI/HDMI
DP_X_L0	TX_x_D2
DP_X_L0#	TX_x_D2#
DP_X_L1	TX_x_D1
DP_X_L1#	TX_x_D1#
DP_X_L2	TX_x_D0
DP_X_L2#	TX_x_D0#
DP_X_L3	TX_x_CLK
DP_X_L3#	TX_x_CLK#
DP_X_AUX	DDC_x_CLK
DP_X_AUX#	DDC_x_DATA

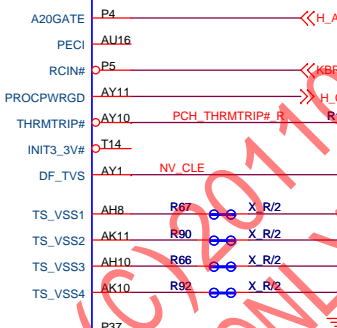
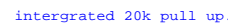
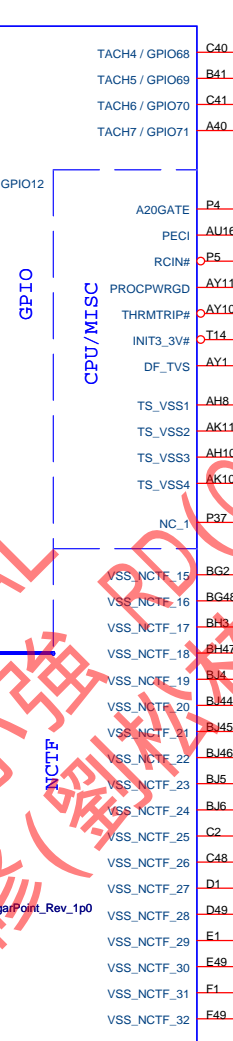
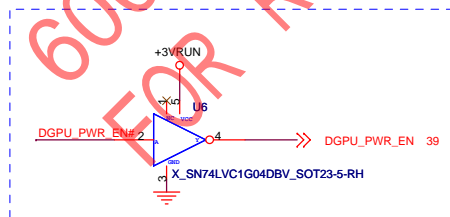
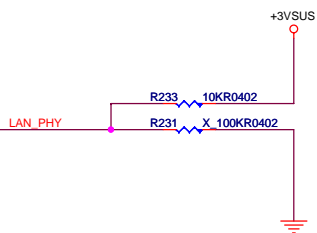
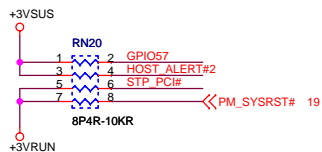
Boot BIOS Strap		
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	—
1	1	SPI



GPIO27 is deep S4 & S5 weak up event, internal pull high. & It's VCCFDIPLL internal VRM strapping pin  
GPIO35 --Un- Muxed. If not used Can be NC

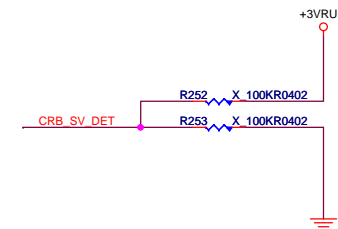
```
+3VRUN TACH[7:0]/GPIO[71:68, 7.6.1.17,27,28] intergrated 20k pull upsummer 443554 P97
```

FDI termination voltage override	
GPIO37	Low-- TX,RX terminated to same voltage (DC coupling mode)default



These signals should not float on the motherboard. They should be tied to GND directly.

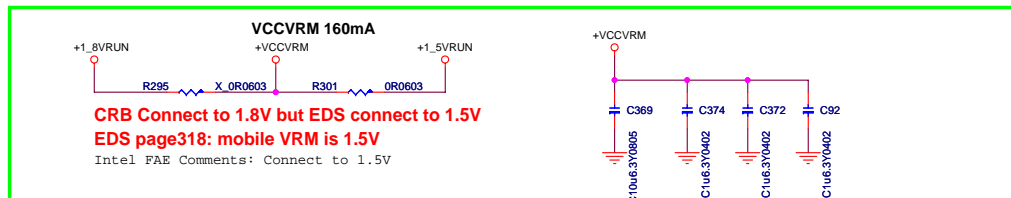
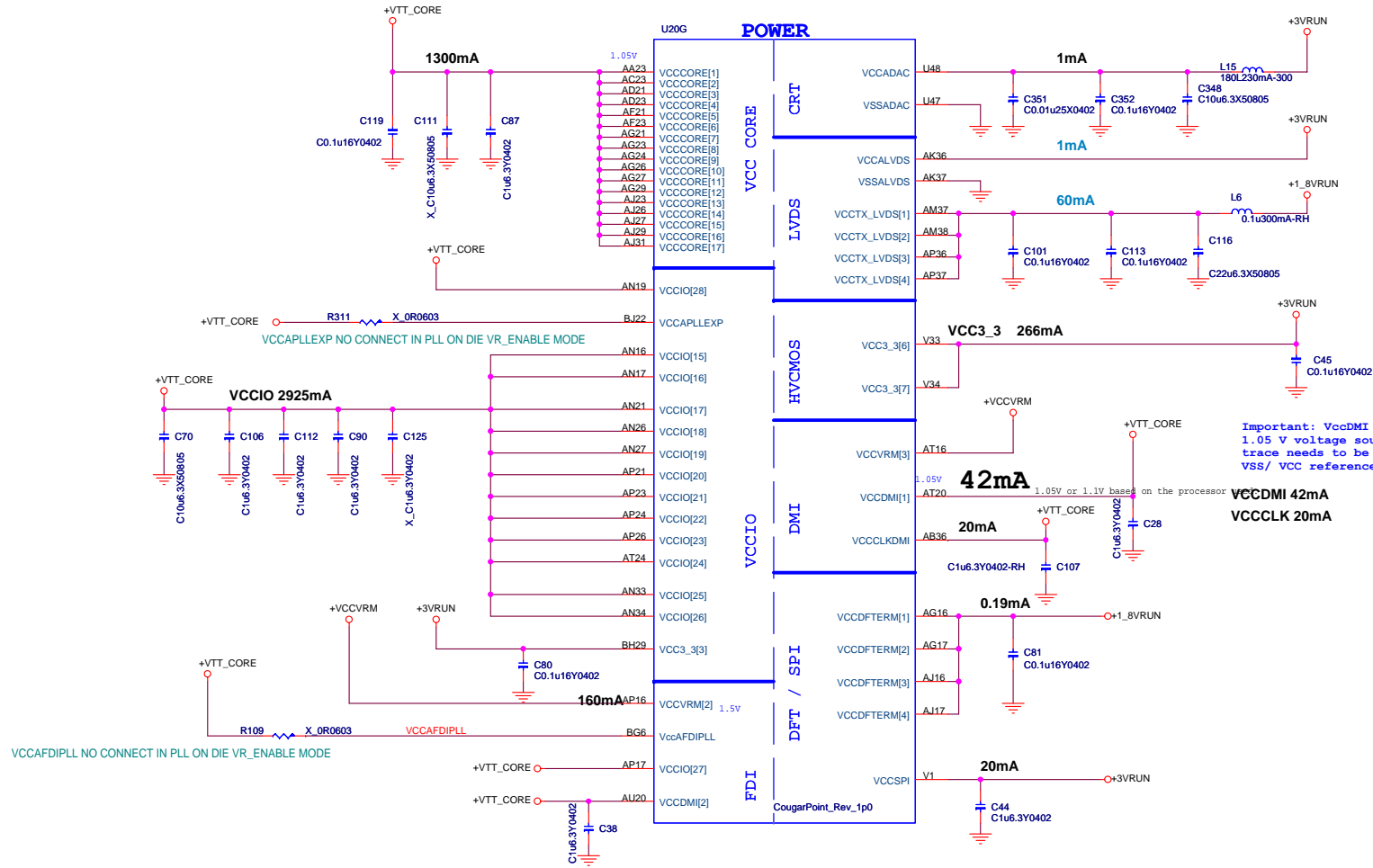
DMI & FDI Termination Voltage	
NV_CLE	Set to VSS when LOW
	Set to VCC when High



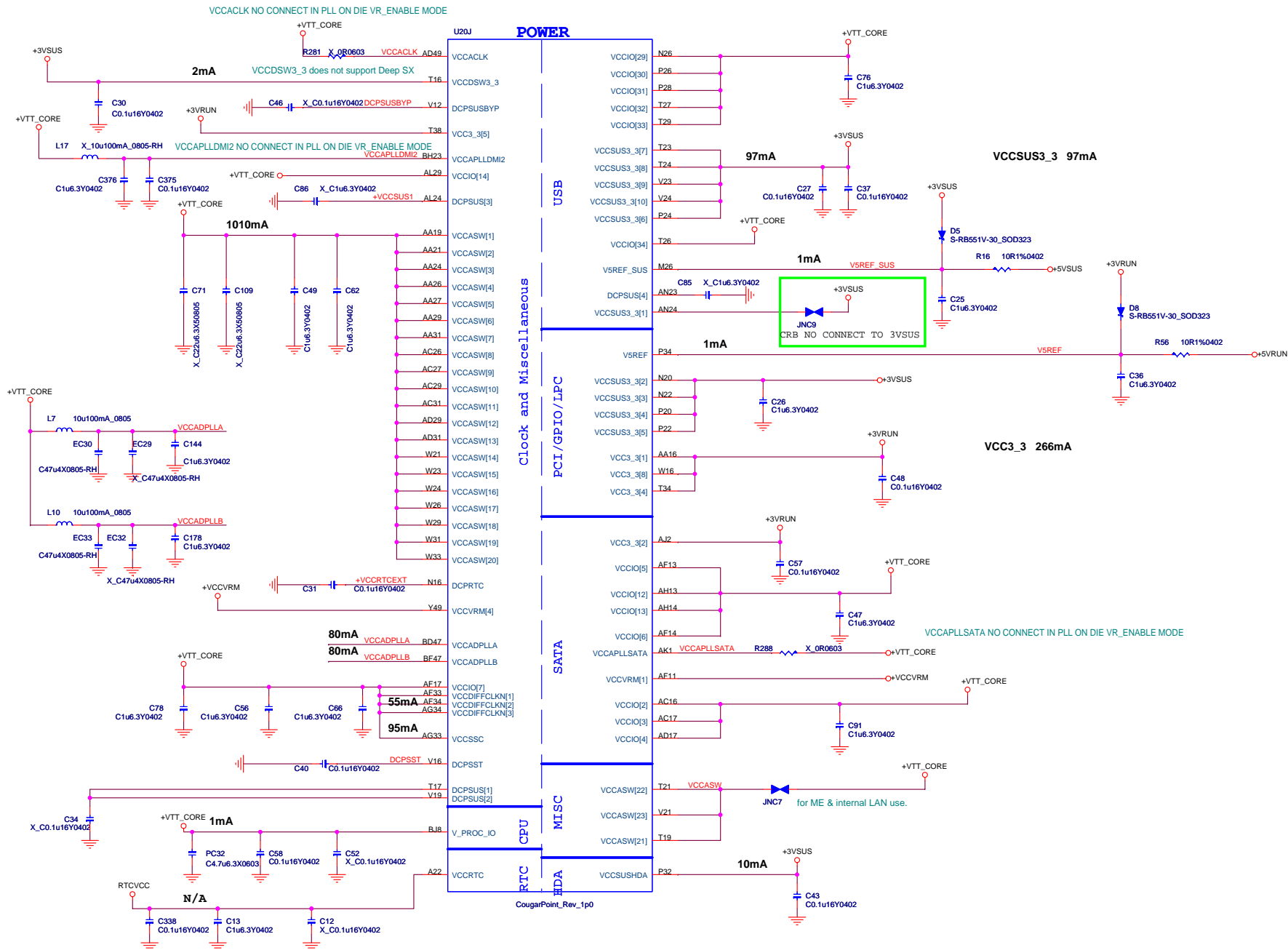
CRB_SV_DET	
GPIO39	High: External GFX
	Low: Internal GFX



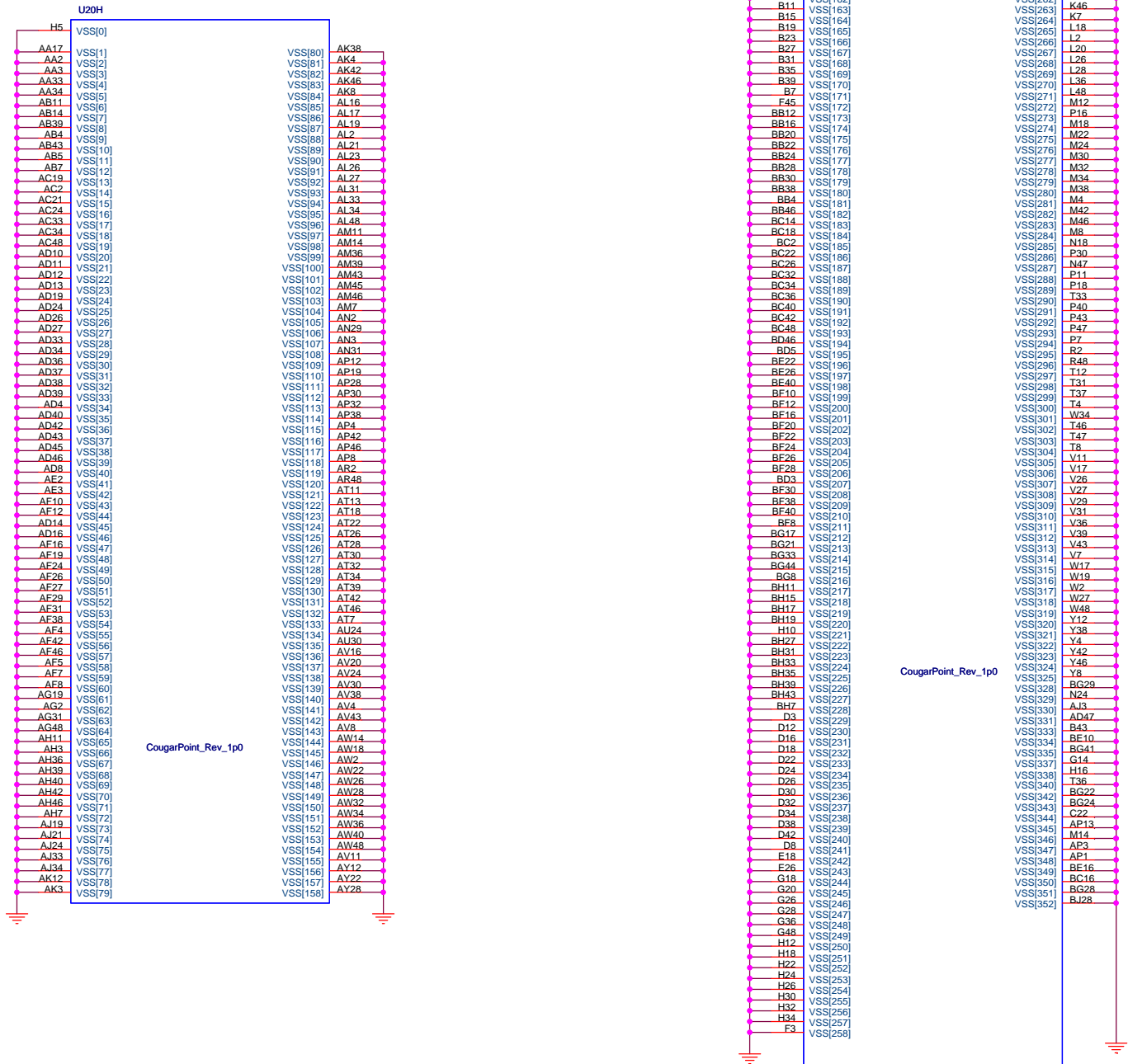
# COUGAR POINT (POWER)

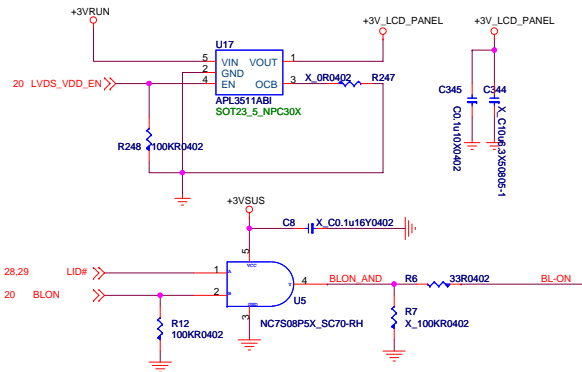


### COUGAR POINT (POWER)



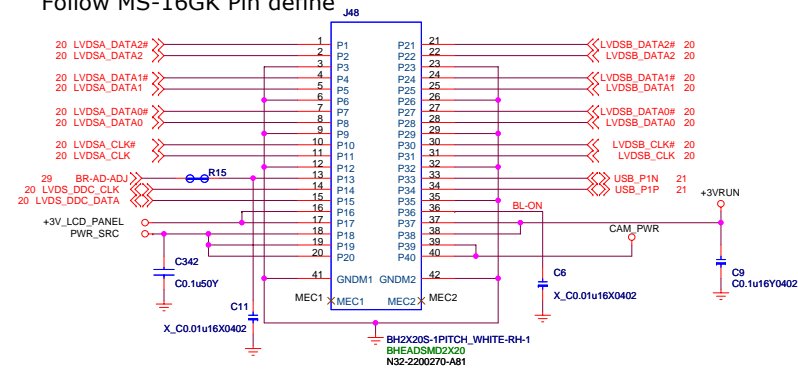
Cougar Point (GND)



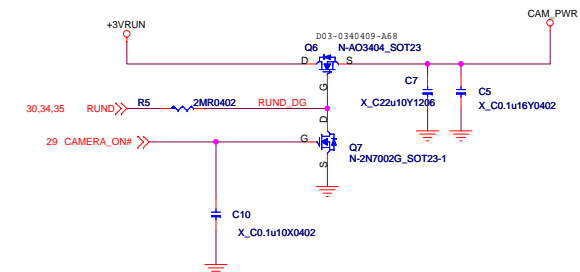


ChA . L  
Follow MS-16GK Pin define

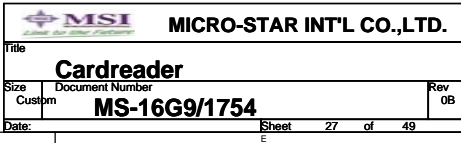
ChB . H

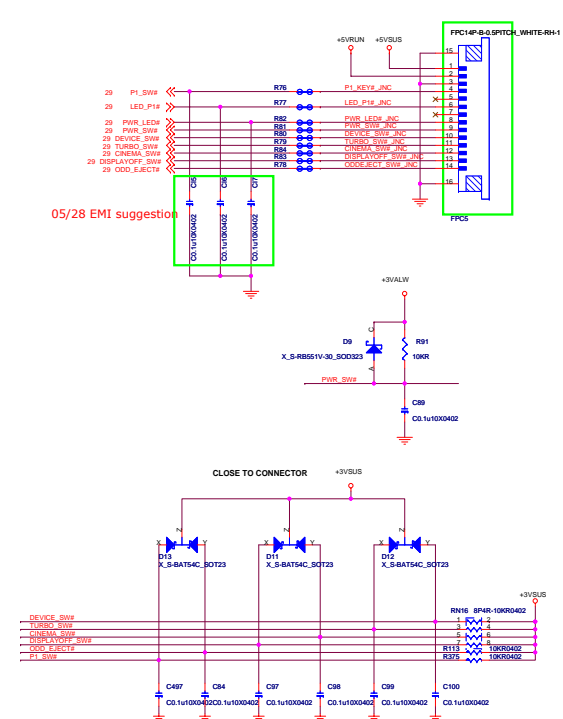
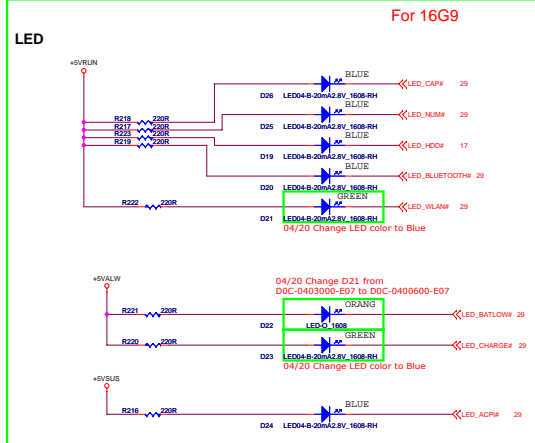
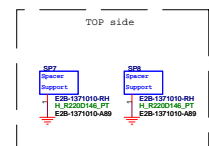
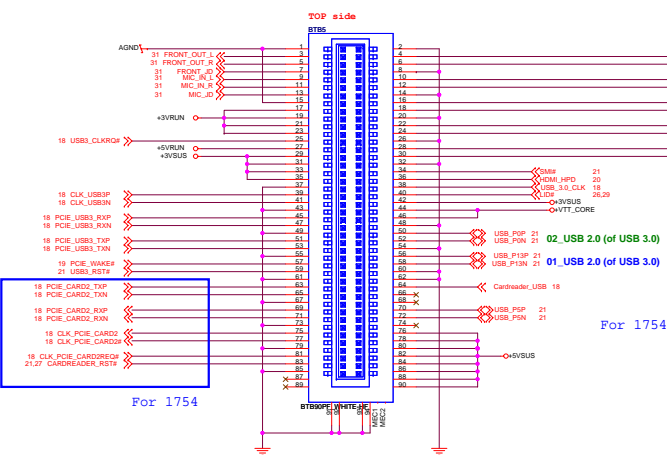


CAMERA LVDS ON

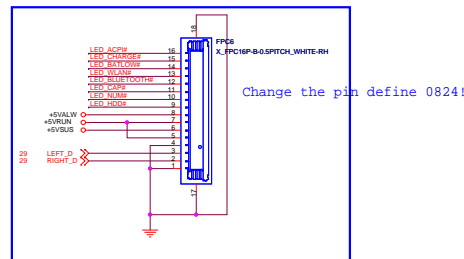


Title			
CRT/LVDS/CCD			
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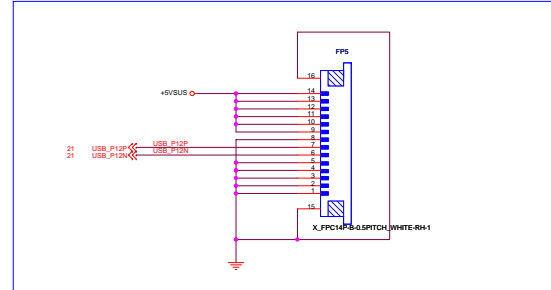




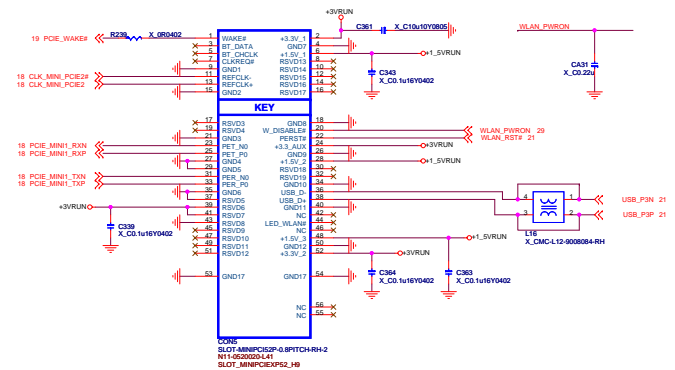
For 1754 E board LED connector

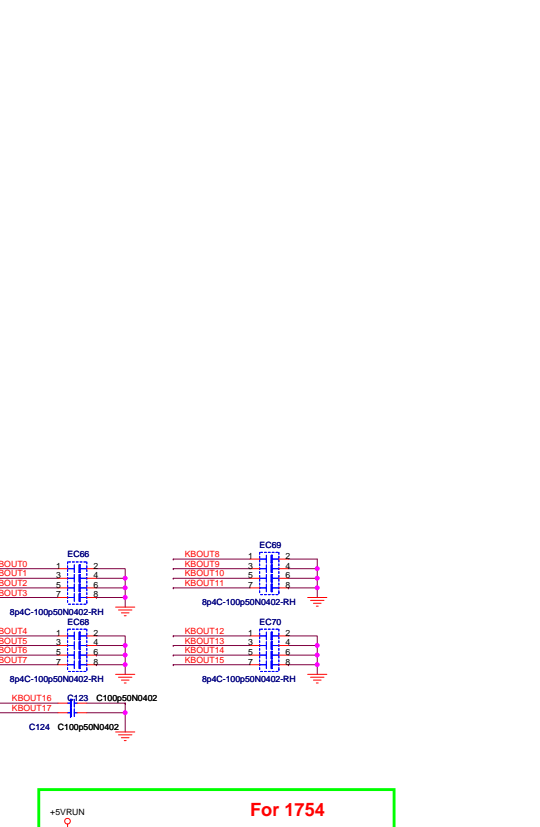


For 1754 D board connector



## WLAN





The diagram illustrates the pin configuration for the 8p4C-100p50N0402-RH component in two views: EC66 and EC69.

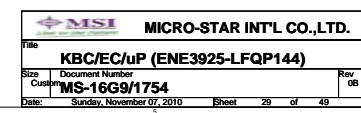
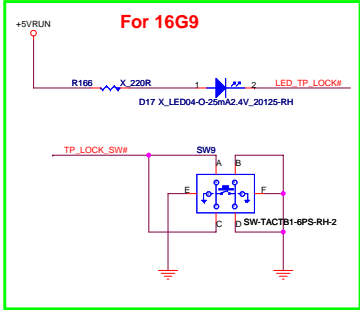
**EC66 View:**

- Pins 1, 2, 3, 4 are on the left side.
- Pins 5, 6, 7, 8 are on the right side.
- Labels: KBOUT0 (1), KBOUT1 (2), KBOUT2 (3), KBOUT3 (4), KBOUT4 (5), KBOUT5 (6), KBOUT6 (7), KBOUT7 (8).
- Ground symbol connected to pin 8.

**EC69 View:**

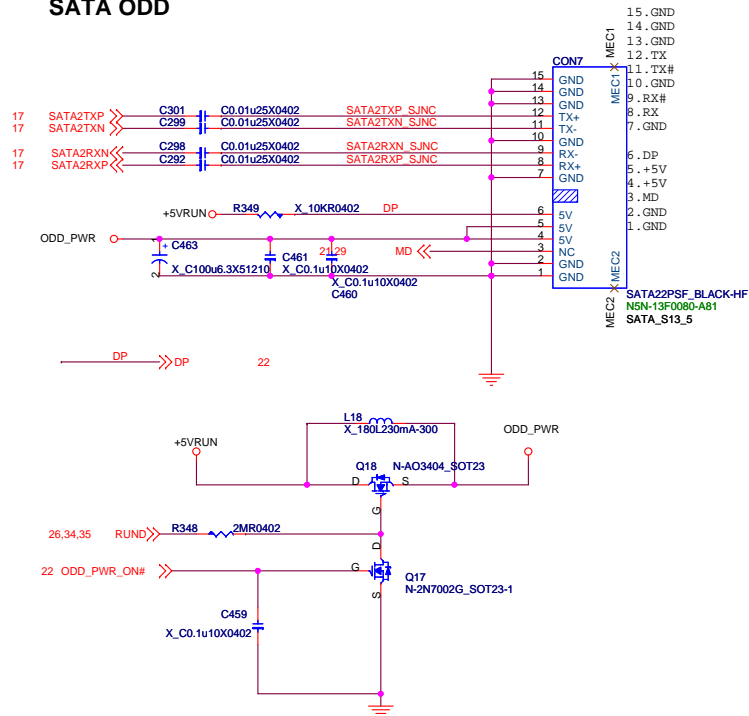
- Pins 1, 2, 3, 4 are on the left side.
- Pins 5, 6, 7, 8 are on the right side.
- Labels: KBOUT12 (1), KBOUT13 (2), KBOUT14 (3), KBOUT15 (4), KBOUT16 (5), KBOUT17 (6), KBOUT18 (7), KBOUT19 (8).
- Ground symbol connected to pin 8.

Schematic diagram of the power supply section of the 1754 module. The diagram shows a transformer with primary taps 1, 2, 3, 4, 5, 6 and secondary taps 7, 8. The secondary is connected to a bridge rectifier (EC70) and a 100p50N0402-RH diode. The output is filtered by a C123 capacitor (100p50N0402) and a C124 capacitor (100p50N0402). The output is labeled +5V/RUN. A note "For 1754" is present. A legend indicates R159 is 220R and LED\_TP\_1 LOCK#.

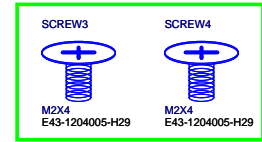
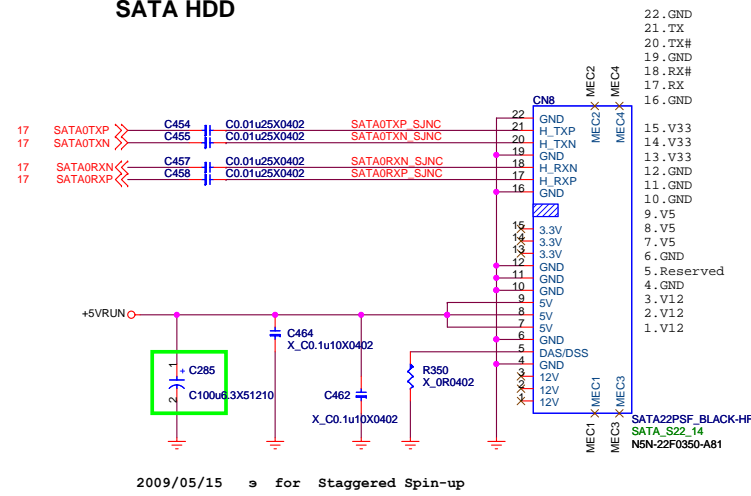




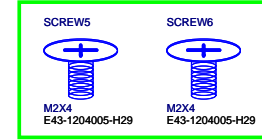
## SATA ODD



## SATA HDD

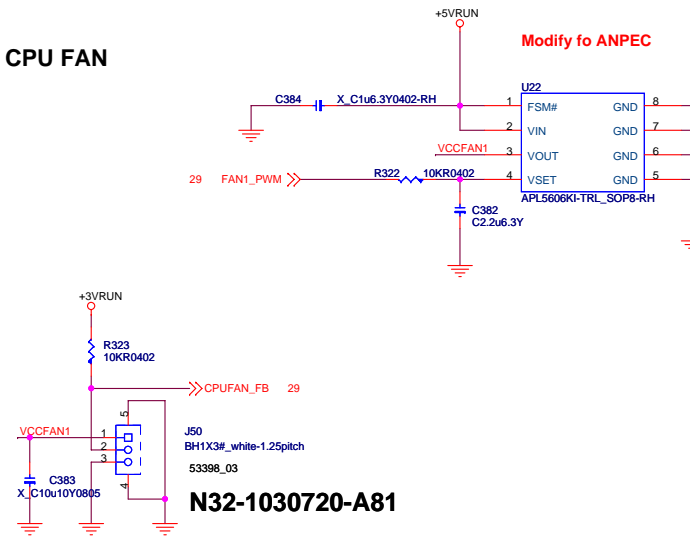


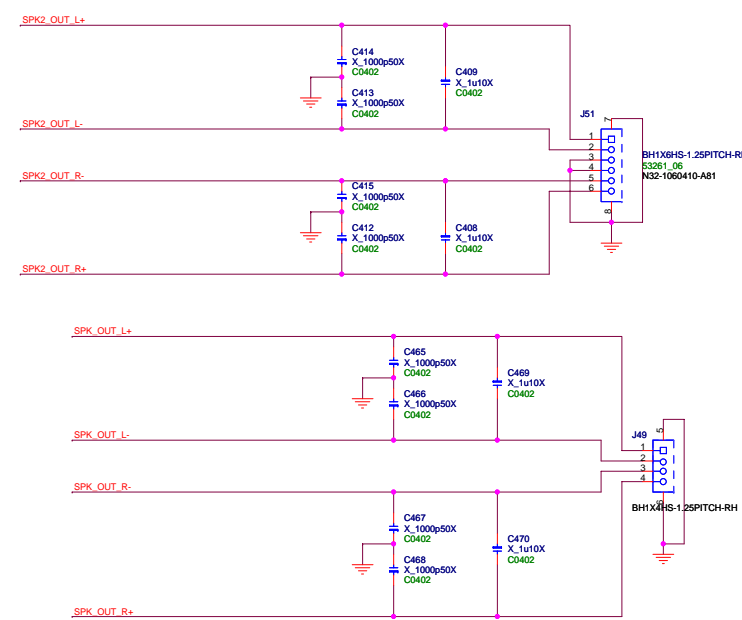
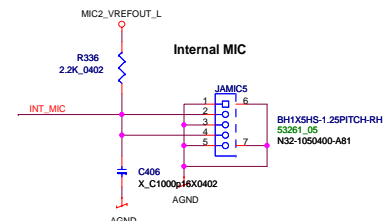
SCREW3, SCREW4 for HDD



SCREW5, SCREW6 for ODD

## CPU FAN

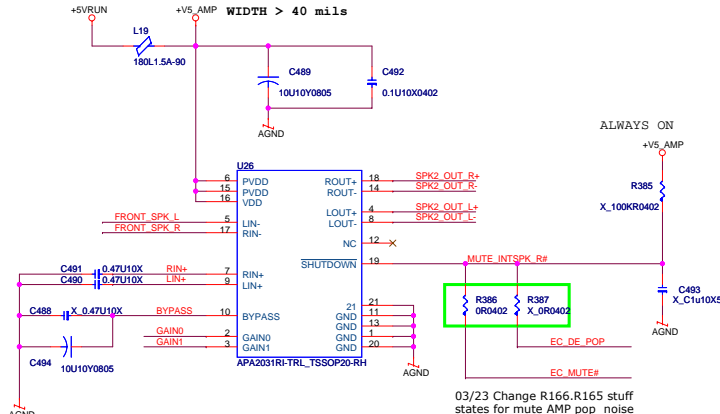




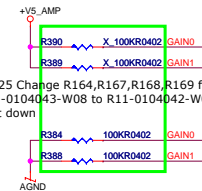
**Speaker wire length is less than 20cm**

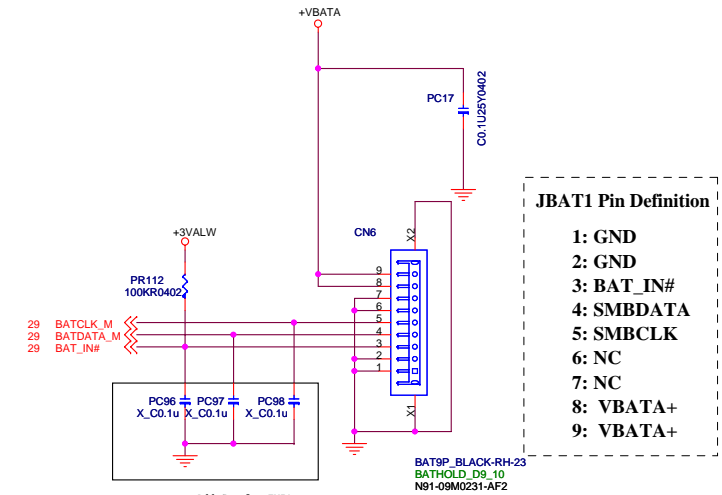
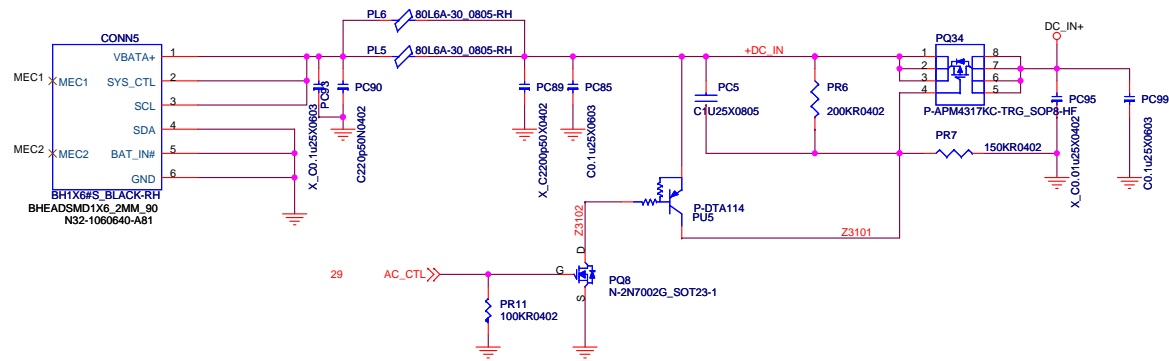
20 mil trace width is required for 40hm loading -----  
10 mil trace width is required for 80hm loading

the trace length/ Speaker wire length of SPKL+/L-/R+/R- is same  
as possible as you can.



For APA2031			For FAN7031			
Av	GAIN0	GAIN1	Av	GAIN0	GAIN1	SE/BTL1
6dB	0	0	6dB	0	0	0
10dB	0	1	10dB	0	1	0
15.6dB	1	0	15.6dB	1	0	0
21.6dB	1	1	21.6dB	1	1	0
4.3dB	X	X	4.3dB	X	X	1



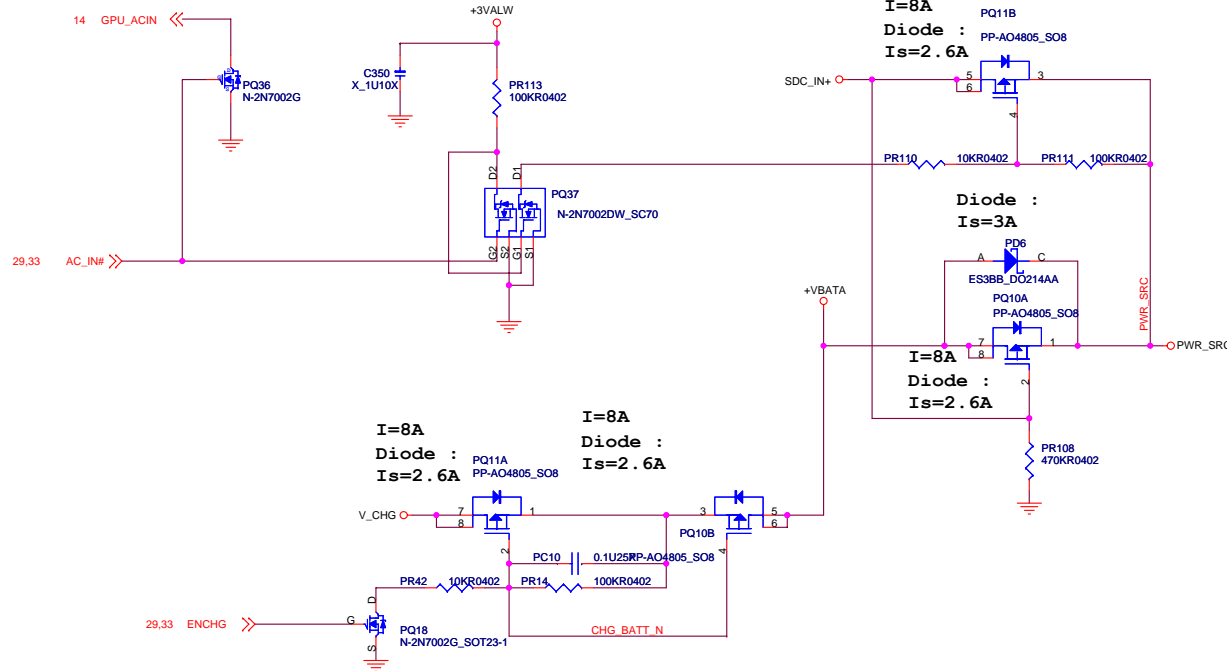


#### JBAT1 Pin Definition

- 1: GND
- 2: GND
- 3: BAT\_IN#
- 4: SMBDATA
- 5: SMBCLK
- 6: NC
- 7: NC
- 8: VBATA+
- 9: VBATA+

BAT9P\_BLACK-RH-23  
BATHOLD\_D9\_10  
N91-09M0231-AF2

Add Cap for EM1!

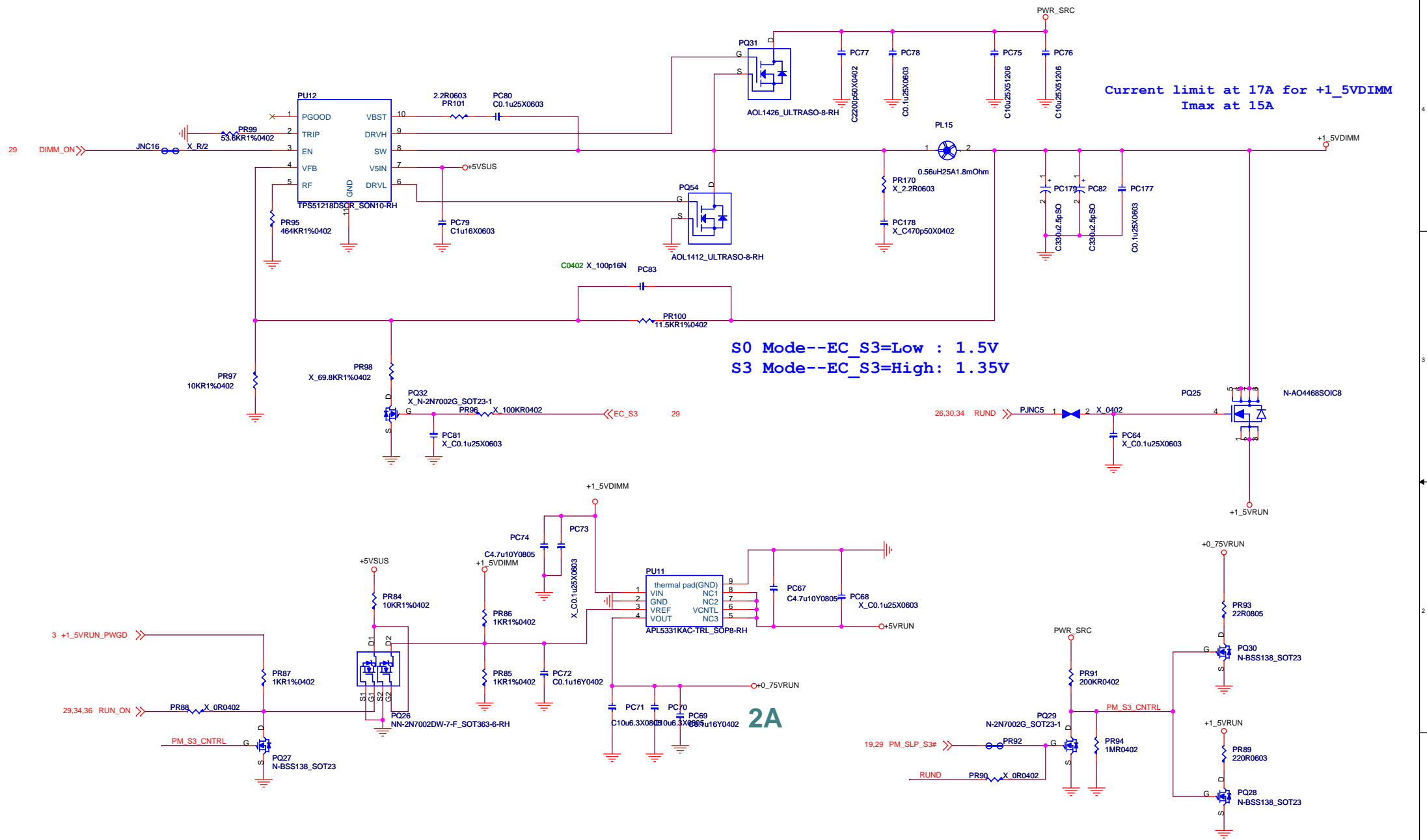




Current limit at 7A for +3VSUS  
Imax at 6A

Current limit at 8A for +5VSUS  
Imax at 7A

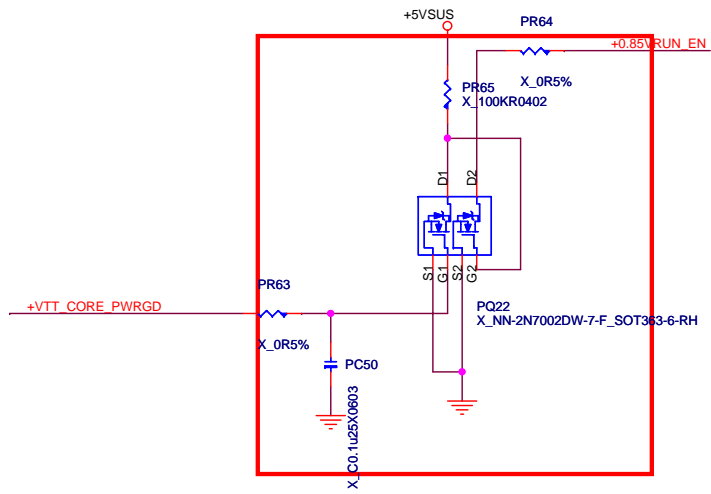
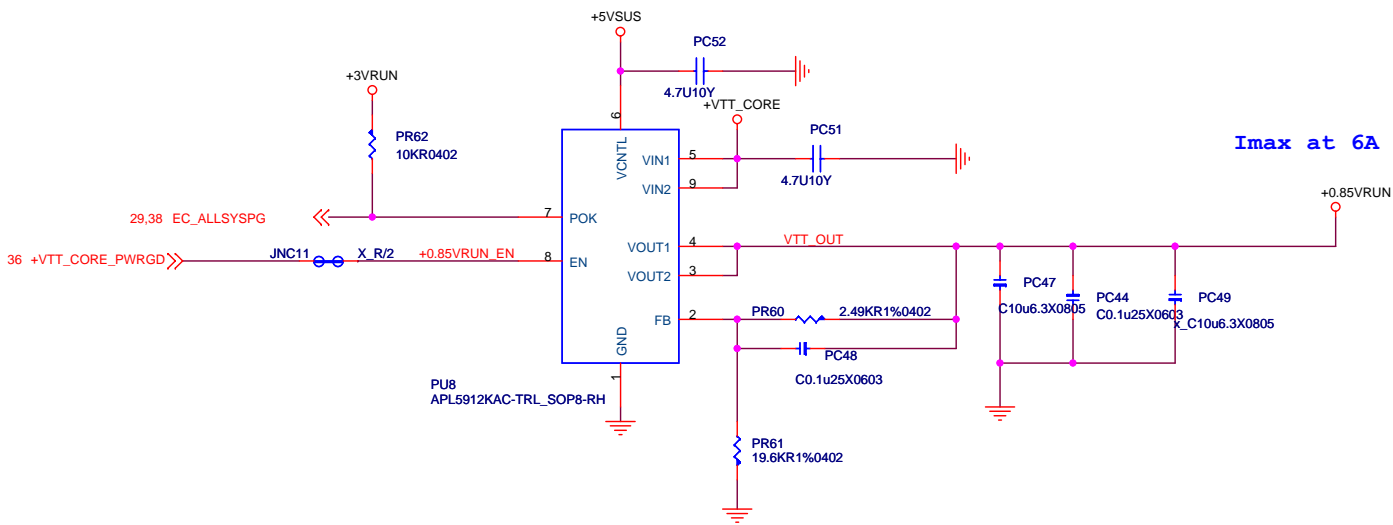
Title		
System Power		
Size	Document Number	Rev
Customer	MS-16G9/1754	08
Date:	Sunday, November 07, 2010	Sheet 34 of 49



Title			DIMM_1.5VRUN
Size	Document Number	Rev	
Customer	MS-16G9/1754	08	
Date:	Sunday, November 07, 2010	Sheet	35 of 49





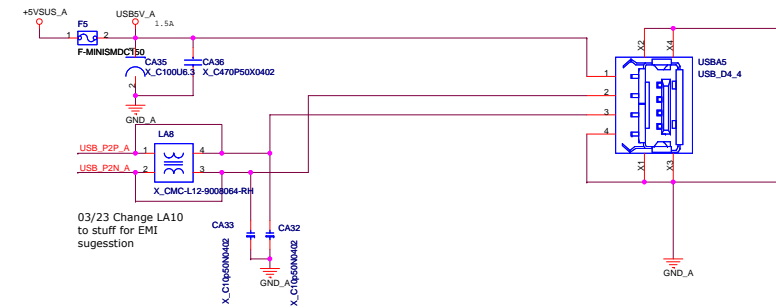
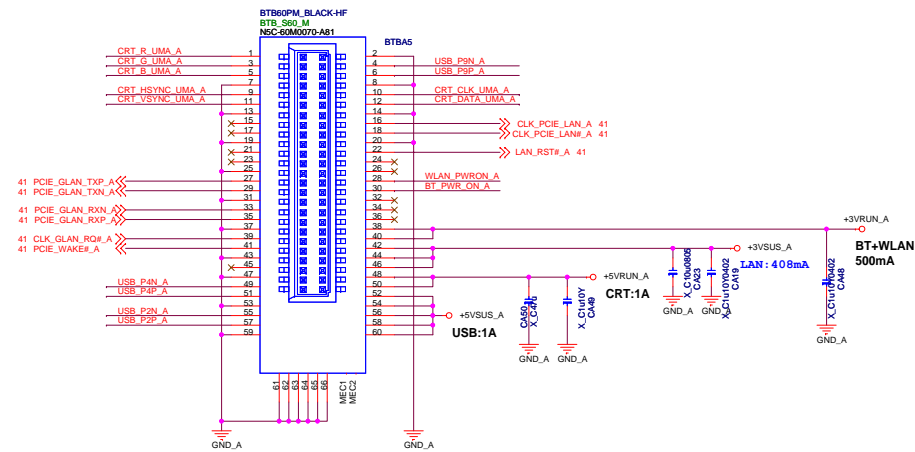


Title			<b>0.85V</b>
Size	Document Number		Rev
B	<b>MS-16G9/1754</b>		0B
Date:	Sunday, November 07, 2010		Sheet 37 of 49



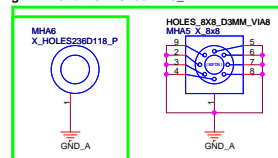


( ESATA,USB,LAN,CRT,BT+WLAN)

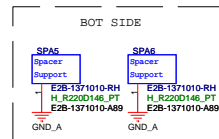


02/25 Change MHA8 to HOLES\_R276D185P\_PT

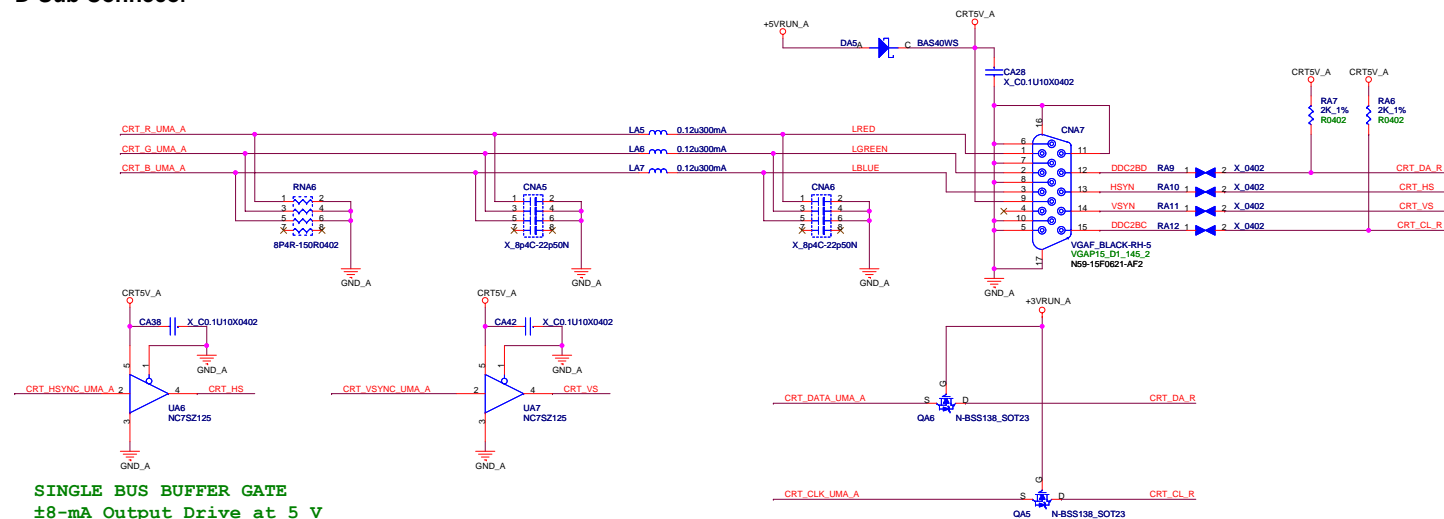
03/30 Change MHA8 to HOLES236D118\_P



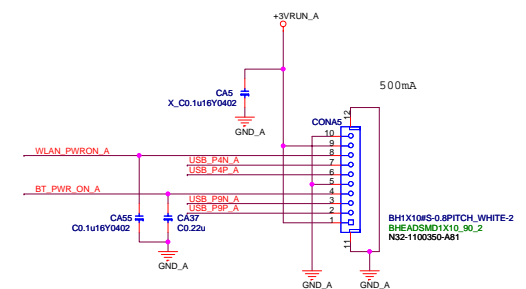
02/23 Change to 8 vias for EMI sugesstion

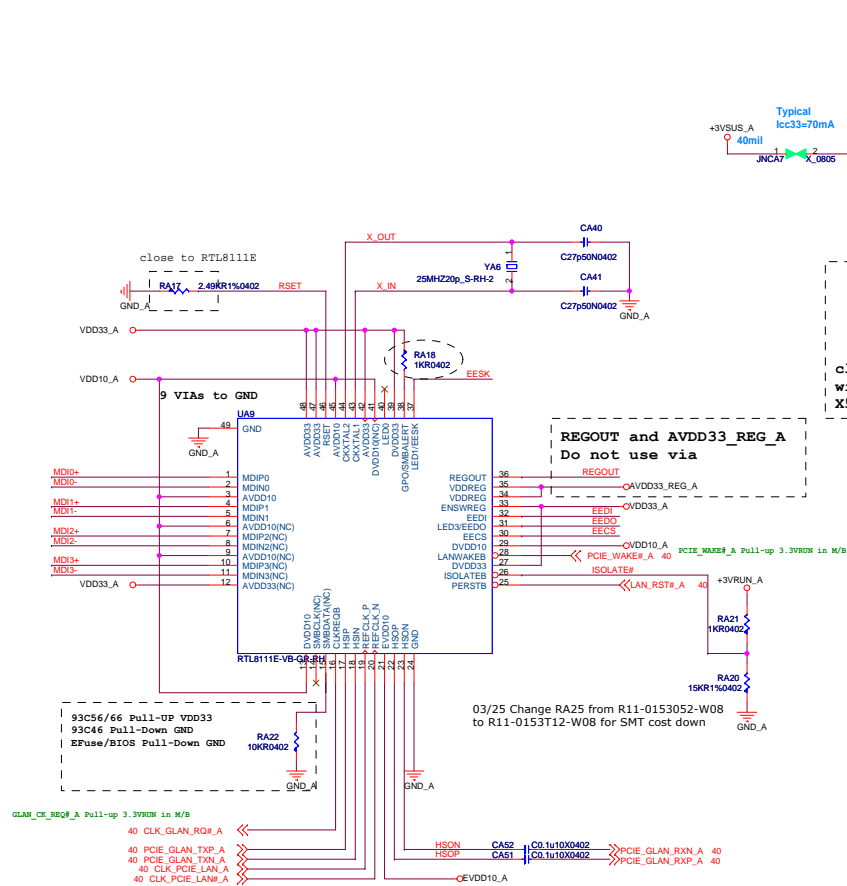


### D-Sub Connector



### BT and WLAN Combo Connector





03/25 Change CA48 to C11-1043062-W08 for SMT cost down

03/25 Change CA49 from C11-4757313-W08 to C11-4757013-M09 for SMT cost down

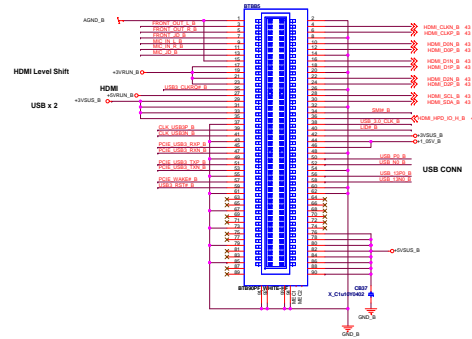
close to p34 p35 within 200mil X5R use

03/24 Change RA18 to NC

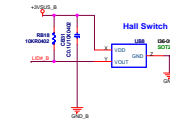
03/24 Change CHOKEA7 to 4.7uH

03/25 Change CA47 to C11-1043062-W08 for SMT cost down

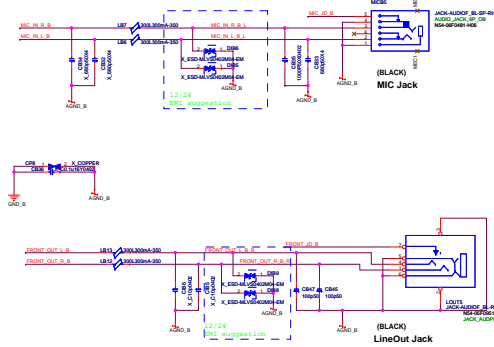
03/25 Change CA46 from C11-4757313-W08 to C11-4757013-M09 for SMT cost down



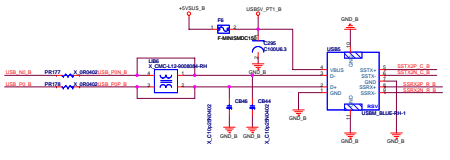
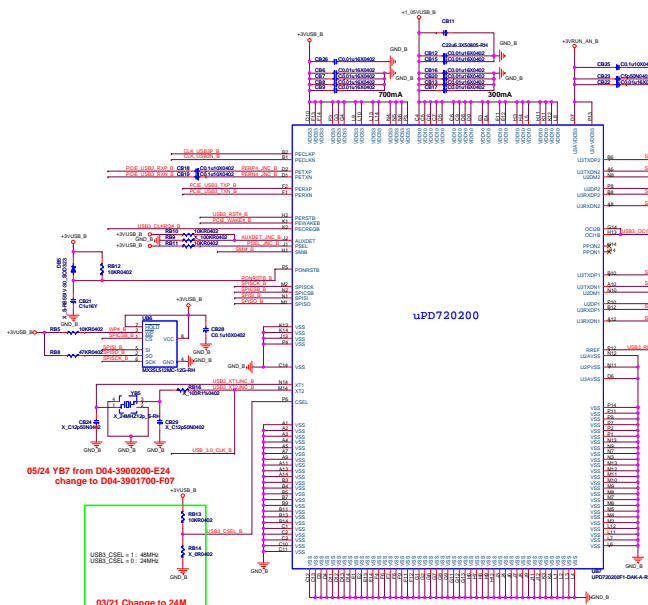
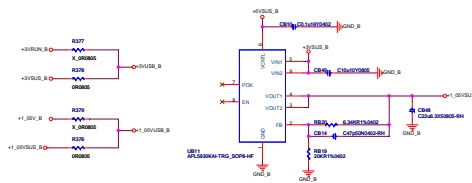
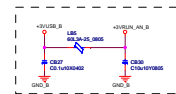
LID Switch



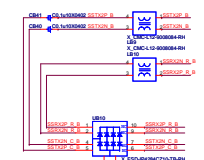
Audio Jack



(※ 四 Card reader, USB 3.0 x 2)  
USB 3.0 Connector

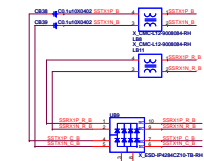


04/14 LB21, LB18 SWAP PIN

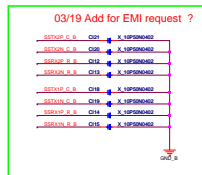


USB2

04/14 LB19, LB20 SWAP PIN



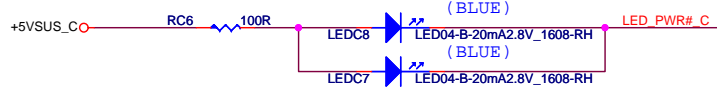
USB1





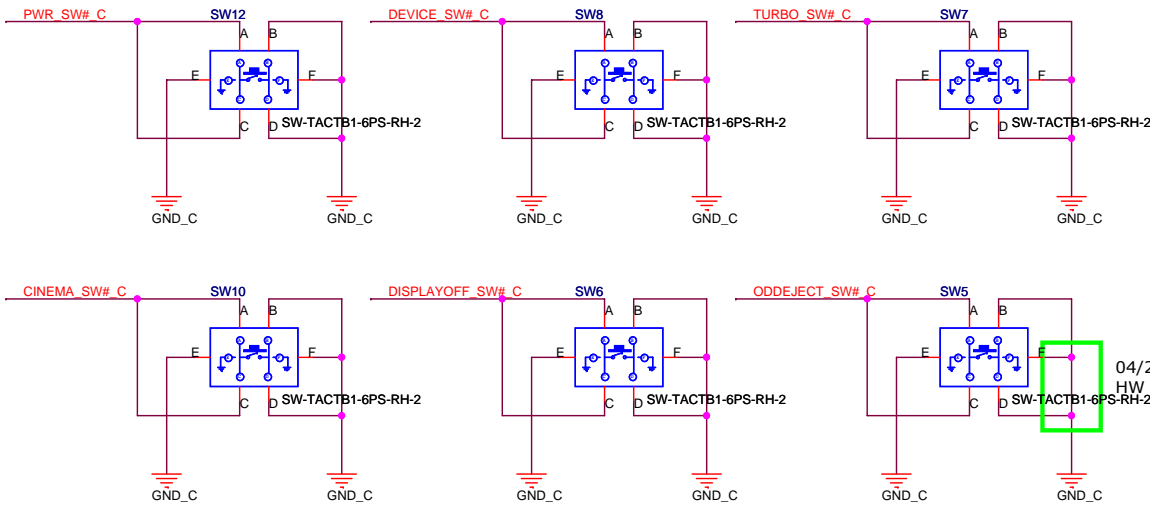


03/30 Change LEDC7.LEDC8 from  
D0C-04018F0-L05 to  
D0C-0400600-E07



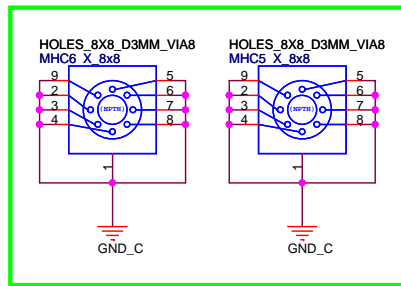
MYLAR22  
POWER\_BOARD  
E2P-6G16211-Y42

03/29 Remove ECO and Cinema LED for ID request

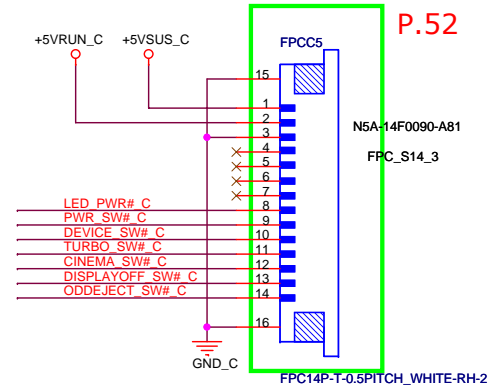


04/28 Fix SWC8's  
HW mismatch

PCBC1  
PCB  
P30-16G9C 0B  
P30-16G9C0B-D05

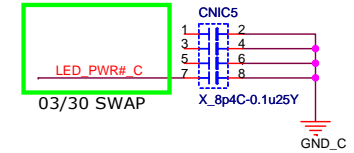


02/10 Add 8 vias for EMI suggestion

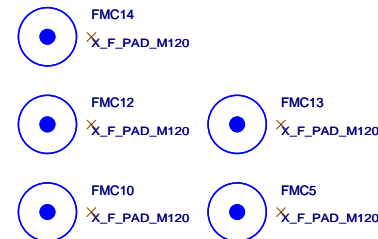
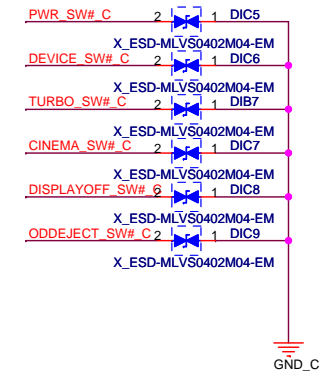
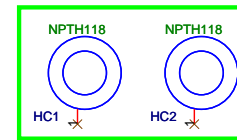



P.52

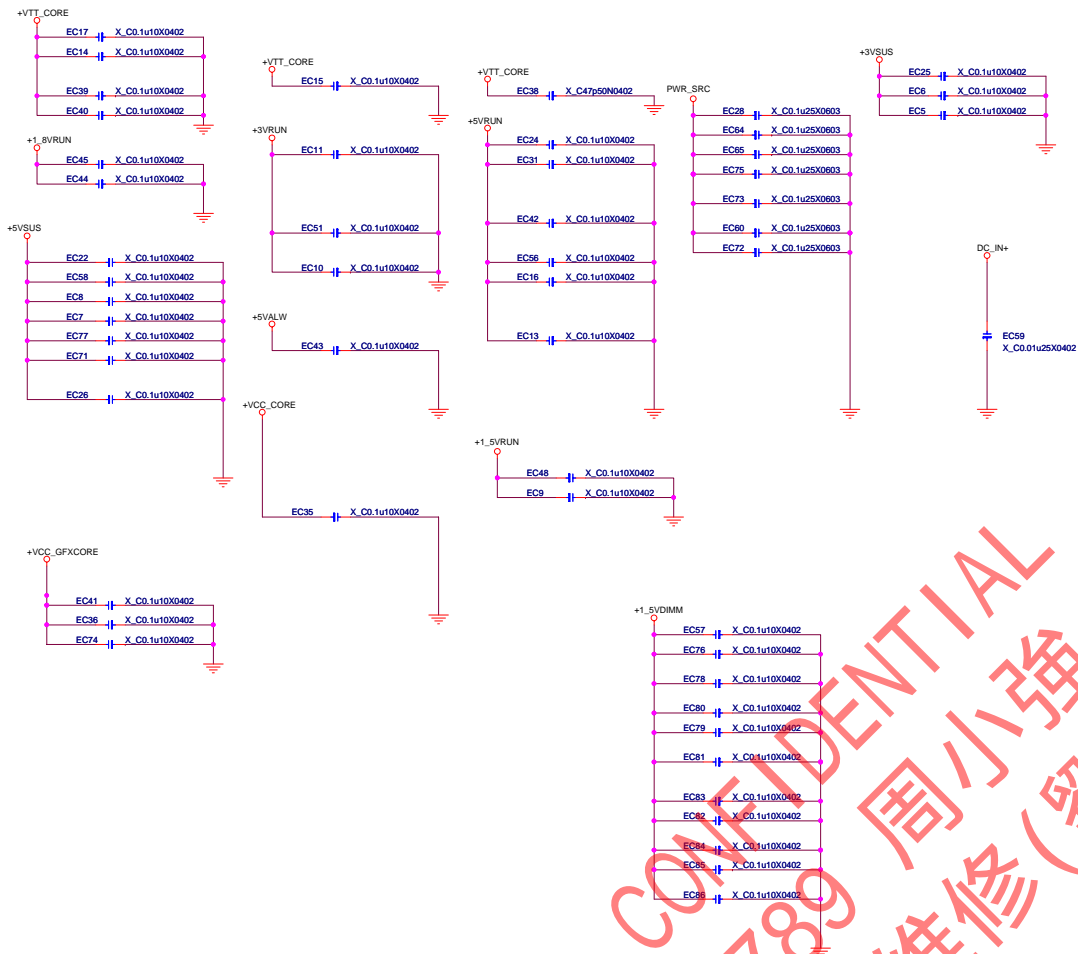
04/23 Change FPC7 from N5A-14F0070-A81 to  
N5A-14F0090-A81(P/N only) for ME request



03/30 SWAP

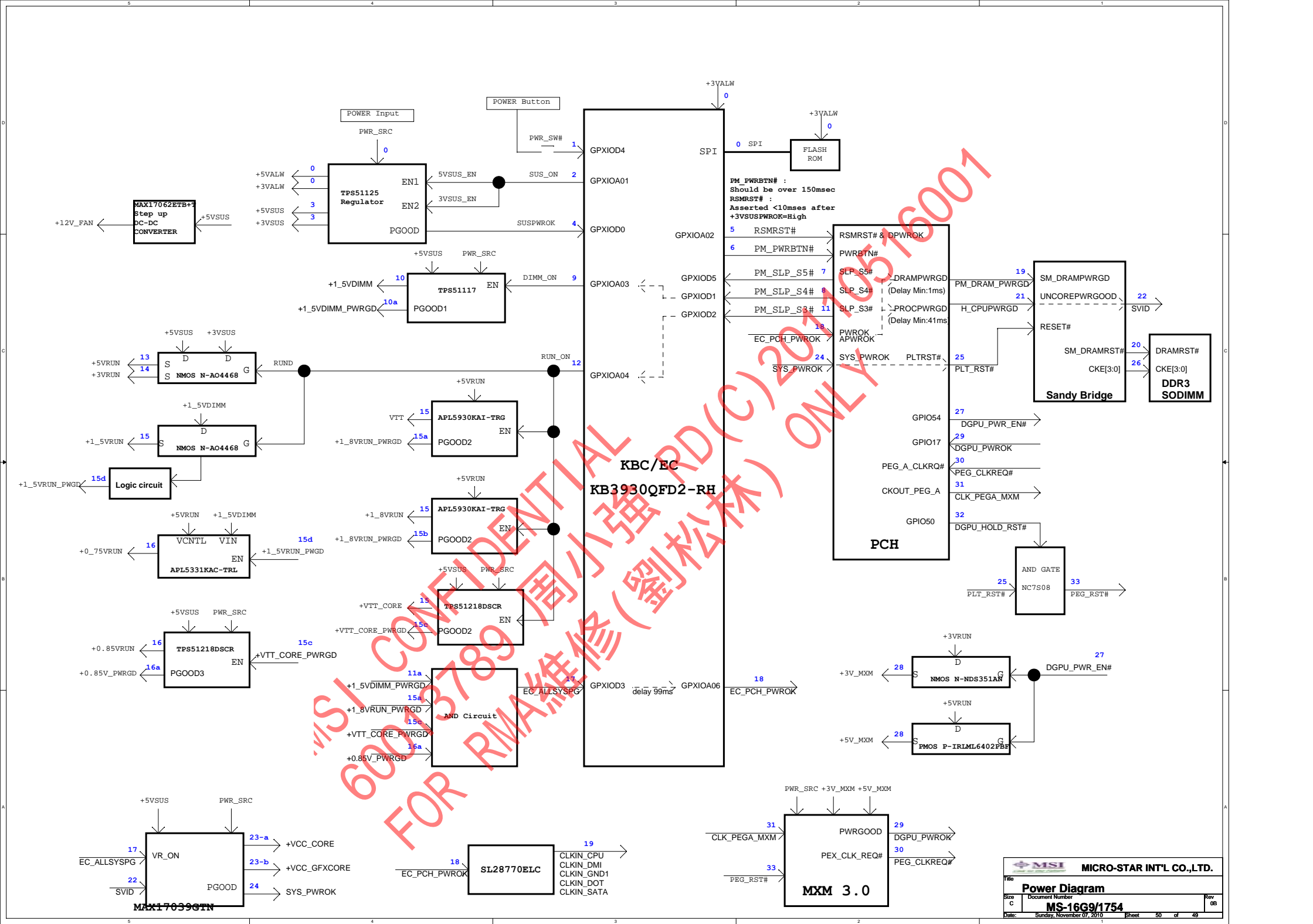


 MICRO-STAR INT'L CO.,LTD.		
Title <b>PWR SW / LED</b>		
Size B	Document Number <b>MS-16G9/1754</b>	Rev 0B
Date:	Sheet 45	of 49



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60013789 周小強 RD(C)20110516001  
FOR RMA維修(劉松林) ONLY

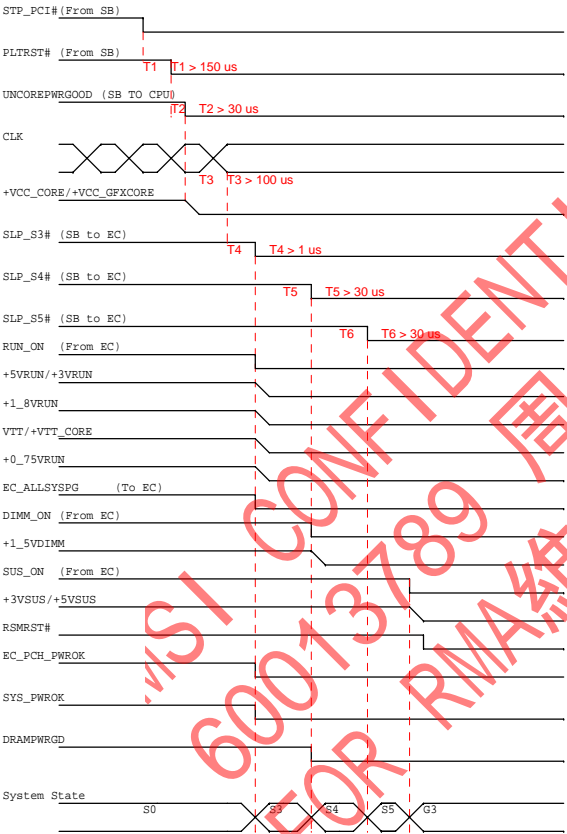




Power down Sequence DC mode S0 to G3

S0-S5

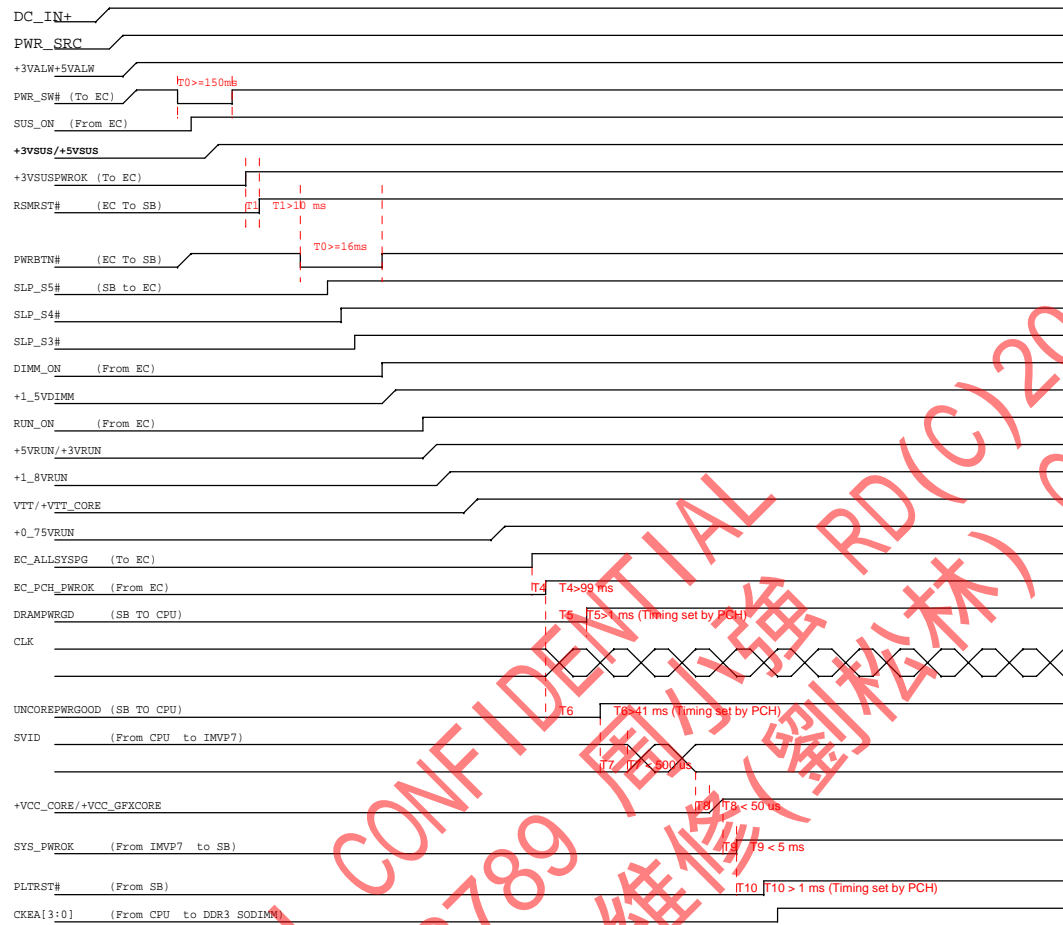
EC programming timing  
Intel Huron River timing SPEC



# S5-S0

EC programming timing

Intel Huron River timing SPEC



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